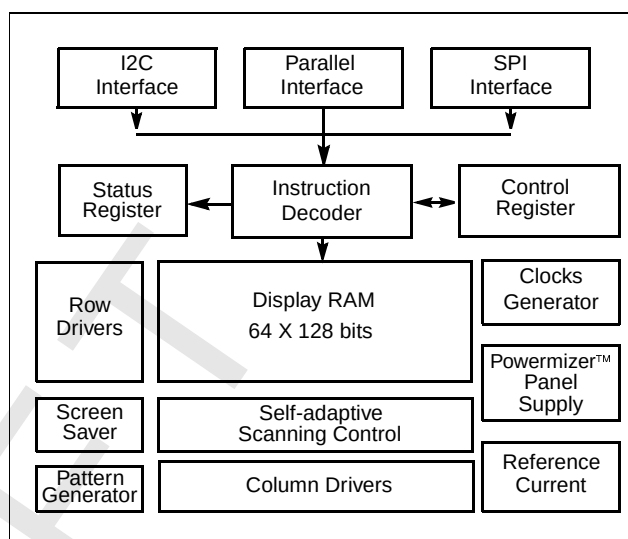


128 x 64 OLED Passive Matrix Controller-Driver

PRODUCT PREVIEW

Main Features

- Support 128 x 64 Dot Matrix Panels
- Embedded DC-DC Step-up Converter
- Display Power Supply up to 20V
- Device Power Supply: 1.8V to 3.3V
- Low-power Consumption Suitable for Battery-operated systems
- Column Source Current: 500µA (max.)
- Row Sink Current: 64mA
- On-chip Oscillator
- Programmable Multiplexing Rate
- Self Adaptive Panel Addressing Scheme
- Powermizer™ Driving Scheme
- Brightness Control with Built-in Aging Compensation
- Built-in Display Pattern Generator
- Selectable 8-bit Parallel Interface (68xx, 80xx series), Serial Peripheral Interface and I²C interface
- Embedded 128 x 64 x 1-bit Graphic RAM
- Row and Column Re-mapping
- Screen Saver Mode
- -40° to +85°C Operating Temperature



Description

The STV8102 is a low-power controller chip for Organic Light Emitting Diode (OLED) dot passive matrix display systems. The STV8102 supports black-and-white monochrome displays with a definition of up to 128 columns and 64 rows.

The STV8102 provides all necessary functions in a single chip, including on-chip OLED supply control and bias current generators, resulting in a minimum of external components and in very low-power consumption.

The STV8102 communicates with the system via fully configurable interfaces (parallel, serial or I²C) to ease interfacing with the host microcontroller. The STV8102 has a set of control and status registers that can be addressed by the interfaces.

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1 General Overview

The STV8102 is a monochrome, black and white, low-power controller from STMicroelectronics' family of controllers for OLED displays. It has been developed to bring a flexible solution to applications and systems based on OLED passive matrixes.

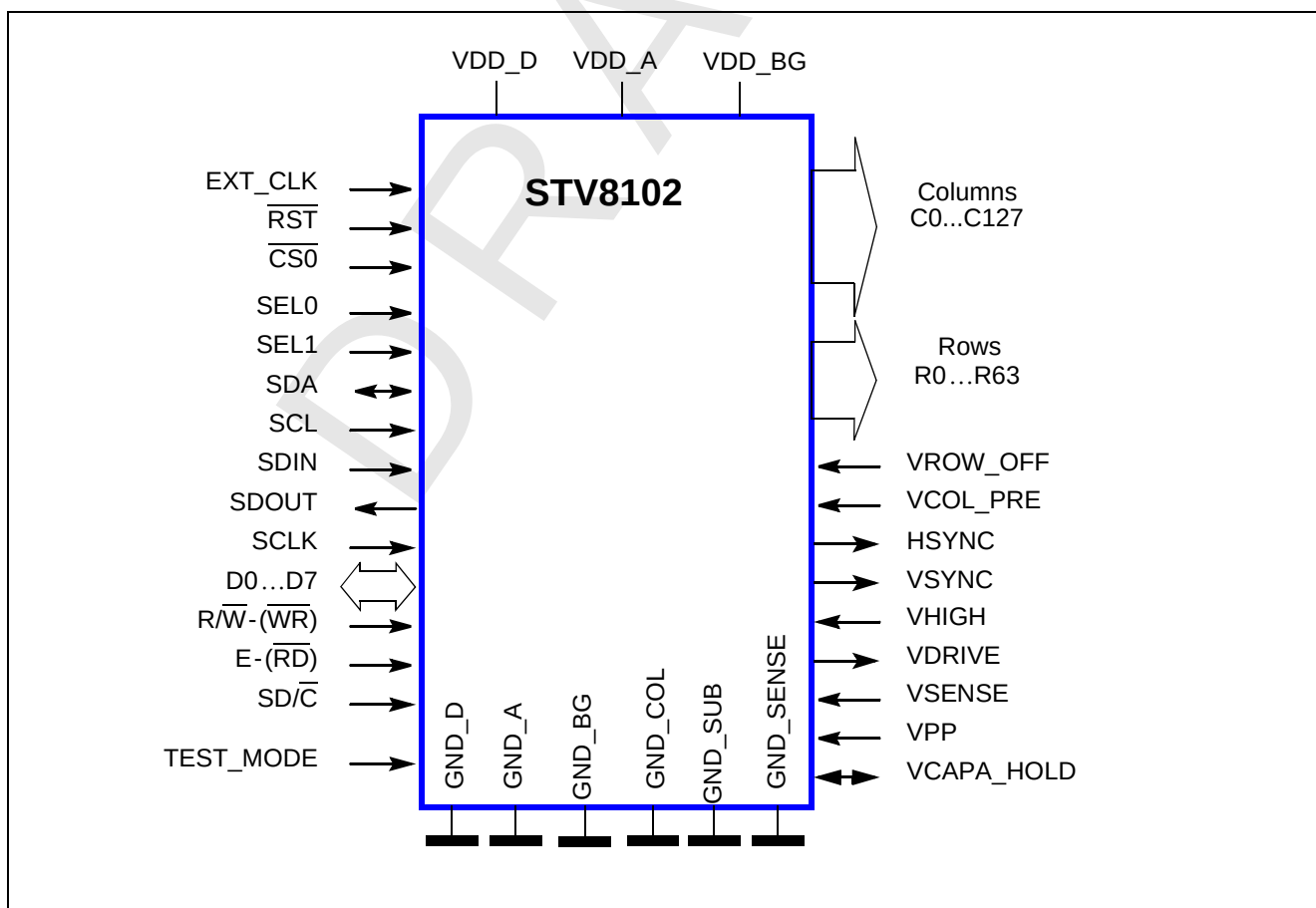
The STV8102 is processed in 0.35µm BCD technology. The supply of the digital core of the controller is typically 3.3V. The controller can operate with a display supply of up to 20V.

The device can be used with many different host microcontrollers. It supports two kinds of serial bus and two parallel interfaces, covering most of the possible application architectures. This provides easy access to the set of status and control registers to properly program the STV8102.

The STV8102 includes a display RAM of 128×64 bits to support the full display capabilities of the 128 column drivers and 64 row drivers with several display functions like mirroring, panning and screen saver. These are described in more detail in [Chapter 4: Display Modes](#).

Processed in BCD technology, the digital core consumes very little power even when the display driver outputs are sourcing 500µA max for executing column commands or sinking 64mA max for row commands. Thanks to a **Powermizer™** supply control and **Self-adaptive Scanning** scheme, total power consumption of the STV8102 fits within the specification of several Nomadic™ applications. With the STV8102, the number of external components is drastically reduced. See [Chapter 5: Display Addressing Scheme](#) and [Chapter 7: Power Supply Management - Powermizer™](#) for more details. Refer [Chapter 11: Electrical Characteristics](#) for the operating ranges and timings of the various parameters and interfaces.

Figure 1: STV8102 Input/Output Diagram



1.1 Bump Die Pad Description

Figure 2: Die Description (Bump-side View)

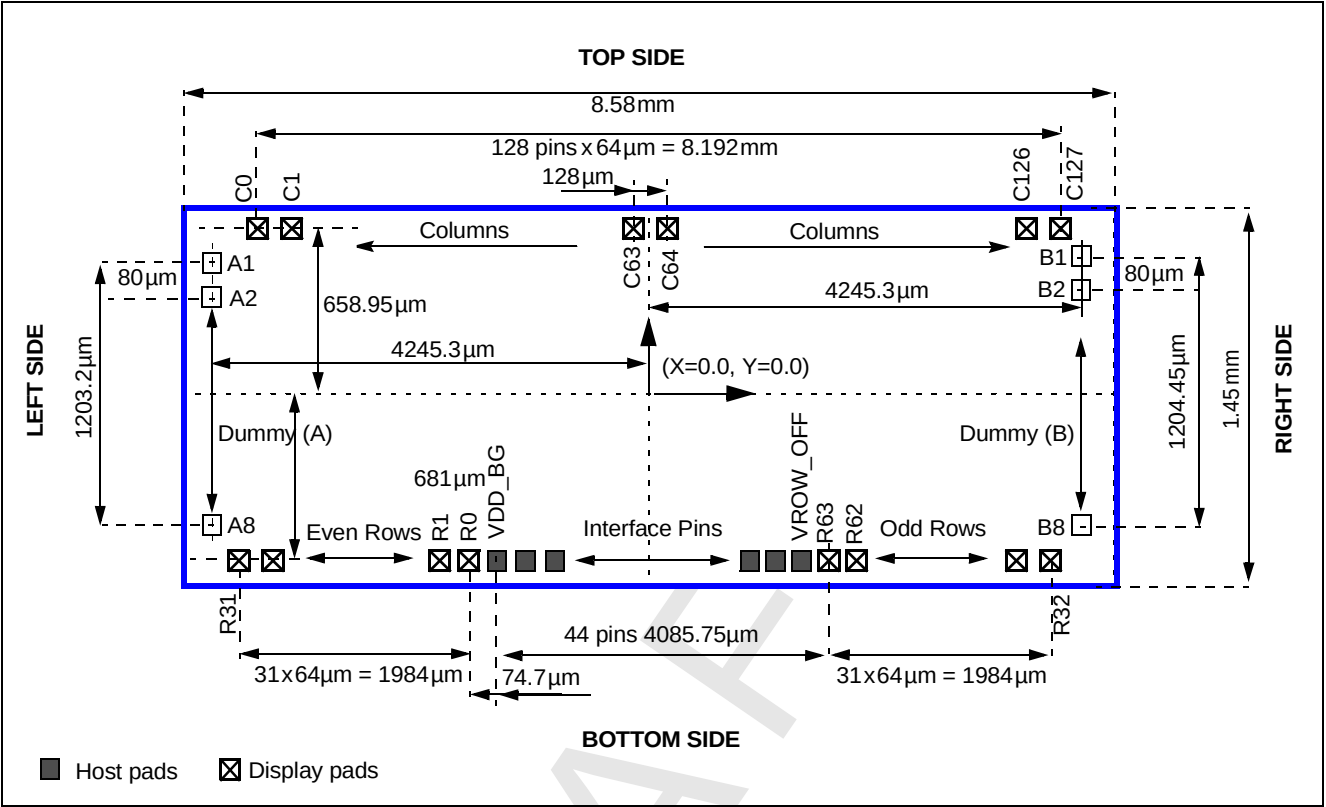
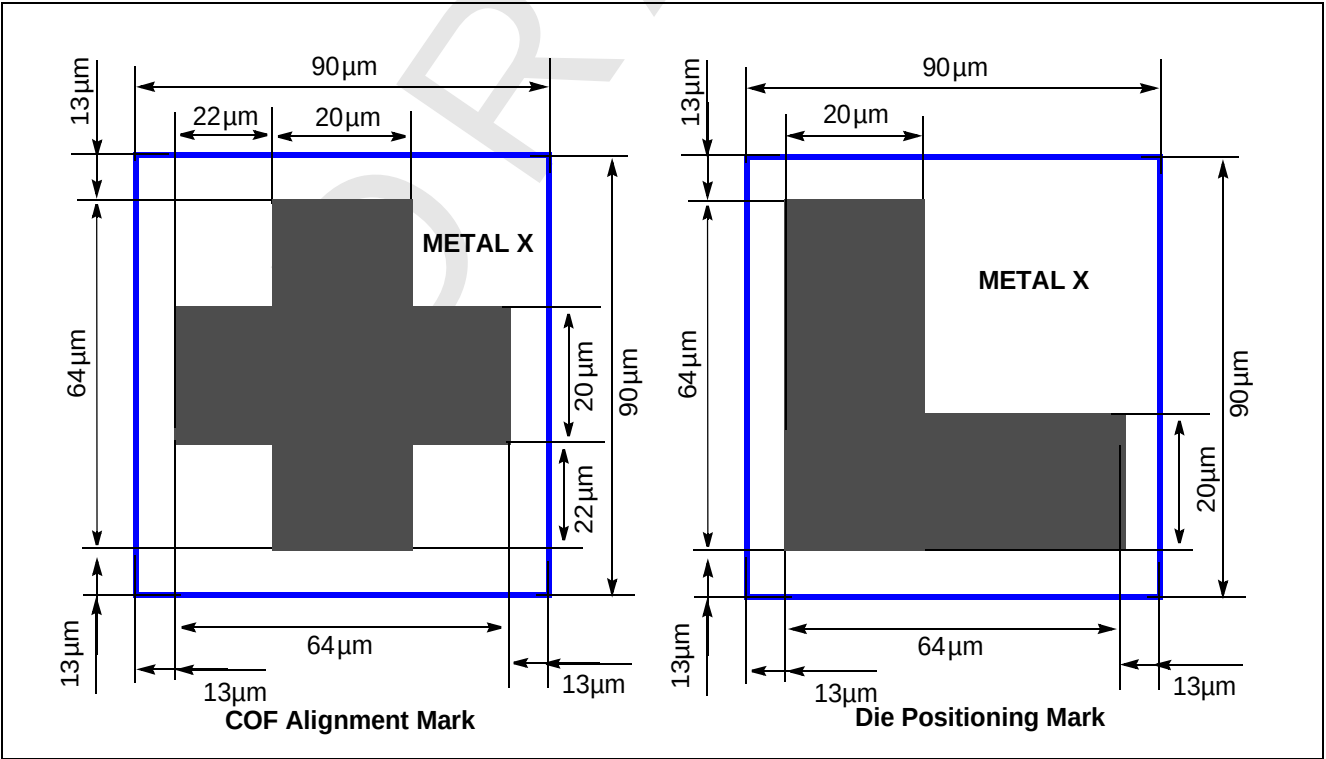


Figure 3: COF Alignment and Die Positioning Marks



1.2 Pad Signal Description

Table 1: STV8102 Pad Description (Sheet 1 of 2)

Ball Name	Input/Output	Description
$\overline{\text{CS0}}$	I	Chip select
$\text{SD}/\overline{\text{C}}$	I	Interface data/command selection
$\text{R}/\overline{\text{W}}-(\overline{\text{WR}})$	I	68XX Parallel interface: read/write or 80XX Parallel interface: write
$\text{E}-(\overline{\text{RD}})$	I	68XX Parallel interface: data enable or 80XX Parallel interface: read
D0 to D7	I/O	Parallel interface 8 bit data bus (bi-directional pins)
SDOUT	O	Serial interface data output
SDIN	I	Serial interface data input
SCLK	I	Serial interface clock
SCL	I	I ² C bus clock
SDA	I/O	I ² C data input/output
$\overline{\text{RST}}$	I	Hardware Reset pin
HSYNC	O	Horizontal synchronization triggering signal
VSYNC	O	Vertical synchronization triggering signal
SEL1	I	Interface mode selection
SEL0	I	Interface mode selection
VDD_D	Supply	Low Voltage Digital Supply
VDD_A	Supply	Low Voltage Analog Supply
VDD_BG	Supply	Low Voltage Reference Supply
GND_D	Supply	Digital Ground
GND_SUB	Supply	Substrate Ground
GND_BG	Supply	Low Voltage Reference Ground
GND_A	Supply	Analog Ground
TEST_MODE	I	Must be grounded
GND_COL	Supply	Analog Ground for Column Driver
GND_SENSE	Supply	Ground of current detection for Step-up Circuitry
VSENSE	I	Current detection of Step-up Circuitry
EXT_CLK	I	External Clock input
VCAPA_HOLD	I	Pre-charge supply filtering
VHIGH	I	High Voltage Step-up Circuit
VDRIVE	O	Control Signal for Output Voltage Generator
VPP	Supply	High voltage Supply for Display Addressing
VCOL_PRE	I	Voltage reference for Column Electrode Pre-charge Sequence
VROW_OFF	I	Voltage reference for row electrode off-mode
C0 to C127	O	OLED Column Driver Output

Table 1: STV8102 Pad Description (Sheet 2 of 2)

Ball Name	Input/Output	Description
R0 to R63	O	OLED Row Driver Output

1.3 Lead Pad Reference Chart

The reference for the following tables is the center of the die (X = 0.0, Y = 0.0)

Table 2: Top Side (from left to right) (Sheet 1 of 4)

Lead Pad Name	Pad Placements (center), μm		Pad Dimensions, μm	
	X	Y	X	Y
COL0	-4095.550	658.95	26.000	60.000
COL1	-4031.550	658.95	26.000	60.000
COL2	-3967.550	658.95	26.000	60.000
COL3	-3903.550	658.95	26.000	60.000
COL4	-3839.550	658.95	26.000	60.000
COL5	-3775.550	658.95	26.000	60.000
COL6	-3711.550	658.95	26.000	60.000
COL7	-3647.550	658.95	26.000	60.000
COL8	-3583.550	658.95	26.000	60.000
COL9	-3519.550	658.95	26.000	60.000
COL10	-3455.550	658.95	26.000	60.000
COL11	-3391.550	658.95	26.000	60.000
COL12	-3327.550	658.95	26.000	60.000
COL13	-3263.550	658.95	26.000	60.000
COL14	-3199.550	658.95	26.000	60.000
COL15	-3135.550	658.95	26.000	60.000
COL16	-3071.550	658.95	26.000	60.000
COL17	-3007.550	658.95	26.000	60.000
COL18	-2943.550	658.95	26.000	60.000
COL19	-2879.550	658.95	26.000	60.000
COL20	-2815.550	658.95	26.000	60.000
COL21	-2751.550	658.95	26.000	60.000
COL22	-2687.550	658.95	26.000	60.000
COL23	-2623.550	658.95	26.000	60.000
COL24	-2559.550	658.95	26.000	60.000
COL25	-2495.550	658.95	26.000	60.000
COL26	-2431.550	658.95	26.000	60.000

Table 2: Top Side (from left to right) (Sheet 2 of 4)

Lead Pad Name	Pad Placements (center), μm		Pad Dimensions, μm	
	X	Y	X	Y
COL27	-2367.550	658.95	26.000	60.000
COL28	-2303.550	658.95	26.000	60.000
COL29	-2239.550	658.95	26.000	60.000
COL30	-2175.550	658.95	26.000	60.000
COL31	-2111.550	658.95	26.000	60.000
COL32	-2047.550	658.95	26.000	60.000
COL33	-1983.550	658.95	26.000	60.000
COL34	-1919.550	658.95	26.000	60.000
COL35	-1855.550	658.95	26.000	60.000
COL36	-1791.550	658.95	26.000	60.000
COL37	-1727.550	658.95	26.000	60.000
COL38	-1663.550	658.95	26.000	60.000
COL39	-1599.550	658.95	26.000	60.000
COL40	-1535.550	658.95	26.000	60.000
COL41	-1471.550	658.95	26.000	60.000
COL42	-1407.550	658.95	26.000	60.000
COL43	-1343.550	658.95	26.000	60.000
COL44	-1279.550	658.95	26.000	60.000
COL45	-1215.550	658.95	26.000	60.000
COL46	-1151.550	658.95	26.000	60.000
COL47	-1087.550	658.95	26.000	60.000
COL48	-1023.550	658.95	26.000	60.000
COL49	-959.550	658.95	26.000	60.000
COL50	-895.550	658.95	26.000	60.000
COL51	-831.550	658.95	26.000	60.000
COL52	-767.550	658.95	26.000	60.000
COL53	-703.550	658.95	26.000	60.000
COL54	-639.550	658.95	26.000	60.000
COL55	-575.550	658.95	26.000	60.000
COL56	-511.550	658.95	26.000	60.000
COL57	-447.550	658.95	26.000	60.000
COL58	-383.550	658.95	26.000	60.000
COL59	-319.550	658.95	26.000	60.000
COL60	-255.550	658.95	26.000	60.000

Table 2: Top Side (from left to right) (Sheet 3 of 4)

Lead Pad Name	Pad Placements (center), μm		Pad Dimensions, μm	
	X	Y	X	Y
COL61	-191.550	658.95	26.000	60.000
COL62	-127.550	658.95	26.000	60.000
COL63	-63.550	658.95	26.000	60.000
COL64	64.450	658.95	26.000	60.000
COL65	128.450	658.95	26.000	60.000
COL66	192.450	658.95	26.000	60.000
COL67	256.450	658.95	26.000	60.000
COL68	320.450	658.95	26.000	60.000
COL69	384.450	658.95	26.000	60.000
COL70	448.450	658.95	26.000	60.000
COL71	512.450	658.95	26.000	60.000
COL72	576.450	658.95	26.000	60.000
COL73	640.450	658.95	26.000	60.000
COL74	704.450	658.95	26.000	60.000
COL75	768.450	658.95	26.000	60.000
COL76	832.450	658.95	26.000	60.000
COL77	896.450	658.95	26.000	60.000
COL78	960.450	658.95	26.000	60.000
COL79	1024.450	658.95	26.000	60.000
COL80	1088.450	658.95	26.000	60.000
COL81	1152.450	658.95	26.000	60.000
COL82	1216.450	658.95	26.000	60.000
COL83	1280.450	658.95	26.000	60.000
COL84	1344.450	658.95	26.000	60.000
COL85	1408.450	658.95	26.000	60.000
COL86	1472.450	658.95	26.000	60.000
COL87	1536.450	658.95	26.000	60.000
COL88	1600.450	658.95	26.000	60.000
COL89	1664.450	658.95	26.000	60.000
COL90	1728.450	658.95	26.000	60.000
COL91	1792.450	658.95	26.000	60.000
COL92	1856.450	658.95	26.000	60.000
COL93	1920.450	658.95	26.000	60.000
COL94	1984.450	658.95	26.000	60.000

Table 2: Top Side (from left to right) (Sheet 4 of 4)

Lead Pad Name	Pad Placements (center), μm		Pad Dimensions, μm	
	X	Y	X	Y
COL95	2048.450	658.95	26.000	60.000
COL96	2112.450	658.95	26.000	60.000
COL97	2176.450	658.95	26.000	60.000
COL98	2240.450	658.95	26.000	60.000
COL99	2304.450	658.95	26.000	60.000
COL100	2368.450	658.95	26.000	60.000
COL101	2432.450	658.95	26.000	60.000
COL102	2496.450	658.95	26.000	60.000
COL103	2560.450	658.95	26.000	60.000
COL104	2624.450	658.95	26.000	60.000
COL105	2688.450	658.95	26.000	60.000
COL106	2752.450	658.95	26.000	60.000
COL107	2816.450	658.95	26.000	60.000
COL108	2880.450	658.95	26.000	60.000
COL109	2944.450	658.95	26.000	60.000
COL110	3008.450	658.95	26.000	60.000
COL111	3072.450	658.95	26.000	60.000
COL112	3136.450	658.95	26.000	60.000
COL113	3200.450	658.95	26.000	60.000
COL114	3264.450	658.95	26.000	60.000
COL115	3328.450	658.95	26.000	60.000
COL116	3392.450	658.95	26.000	60.000
COL117	3456.450	658.95	26.000	60.000
COL118	3520.450	658.95	26.000	60.000
COL119	3584.450	658.95	26.000	60.000
COL120	3648.450	658.95	26.000	60.000
COL121	3712.450	658.95	26.000	60.000
COL122	3776.450	658.95	26.000	60.000
COL123	3840.450	658.95	26.000	60.000
COL124	3904.450	658.95	26.000	60.000
COL125	3968.450	658.95	26.000	60.000
COL126	4032.450	658.95	26.000	60.000
COL127	4096.450	658.95	26.000	60.000

Table 3: Right Side (from top to bottom)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
DUMMY_B1	4245.300	600	60.000	26.000
DUMMY_B2	4245.300	520	60.000	26.000
DUMMY_B3	4245.300	60.65	60.000	26.000
DUMMY_B4	4245.300	-3.35	60.000	26.000
DUMMY_B5	4245.300	-67.35	60.000	26.000
DUMMY_B6	4245.300	-131.35	60.000	26.000
DUMMY_B7	4245.300	-540.45	60.000	26.000
DUMMY_B8	4245.300	-604.45	60.000	26.000

Table 4: Bottom Side (from right to left) (Sheet 1 of 4)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
ROW32	4096.950	-681	26.000	60.000
ROW33	4032.950	-681	26.000	60.000
ROW34	3968.950	-681	26.000	60.000
ROW35	3904.950	-681	26.000	60.000
ROW36	3840.950	-681	26.000	60.000
ROW37	3776.950	-681	26.000	60.000
ROW38	3712.950	-681	26.000	60.000
ROW39	3648.950	-681	26.000	60.000
ROW40	3584.950	-681	26.000	60.000
ROW41	3520.950	-681	26.000	60.000
ROW42	3456.950	-681	26.000	60.000
ROW43	3392.950	-681	26.000	60.000
ROW44	3328.950	-681	26.000	60.000
ROW45	3264.950	-681	26.000	60.000
ROW46	3200.950	-681	26.000	60.000
ROW47	3136.950	-681	26.000	60.000
ROW48	3072.950	-681	26.000	60.000
ROW49	3008.950	-681	26.000	60.000
ROW50	2944.950	-681	26.000	60.000
ROW51	2880.950	-681	26.000	60.000
ROW52	2816.950	-681	26.000	60.000

Table 4: Bottom Side (from right to left) (Sheet 2 of 4)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
ROW53	2752.950	-681	26.000	60.000
ROW54	2688.950	-681	26.000	60.000
ROW55	2624.950	-681	26.000	60.000
ROW56	2560.950	-681	26.000	60.000
ROW57	2496.950	-681	26.000	60.000
ROW58	2432.950	-681	26.000	60.000
ROW59	2368.950	-681	26.000	60.000
ROW60	2304.950	-681	26.000	60.000
ROW61	2240.950	-681	26.000	60.000
ROW62	2176.950	-681	26.000	60.000
ROW63	2112.950	-681	26.000	60.000
VROW_OFF	2048.950	-681	26.000	60.000
VROW_OFF	1984.950	-681	26.000	60.000
VCOL_PRE	1920.950	-681	26.000	60.000
VCOL_PRE	1856.950	-681	26.000	60.000
VPP	1792.950	-681	26.000	60.000
VPP	1728.950	-681	26.000	60.000
VDRIVE	1664.950	-681	26.000	60.000
VHIGH	1540.700	-681	26.000	60.000
VCAPA_HOLD	1476.700	-681	26.000	60.000
EXT_CLK	1376.700	-681	26.000	60.000
VSENSE	1274.700	-681	26.000	60.000
GND_SENSE	1168.700	-681	26.000	60.000
GND_COL	1064.900	-681	26.000	60.000
TEST_MODE	964.850	-681	26.000	60.000
GND_A	844.350	-681	26.000	60.000
GND_S	780.350	-681	26.000	60.000
GND_D	663.250	-681	26.000	60.000
GND_D	563.200	-681	26.000	60.000
GND_BG	463.200	-681	26.000	60.000
VDD_A	363.200	-681	26.000	60.000
VDD_D	263.200	-681	26.000	60.000
SEL0	163.200	-681	26.000	60.000
SEL1	63.200	-681	26.000	60.000

Table 4: Bottom Side (from right to left) (Sheet 3 of 4)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
VSYNC	-36.800	-681	26.000	60.000
HSYNC	-136.800	-681	26.000	60.000
$\overline{\text{RST}}$	-236.800	-681	26.000	60.000
SDA	-336.800	-681	26.000	60.000
SCL	-436.800	-681	26.000	60.000
SCLK	-536.800	-681	26.000	60.000
SDIN	-636.800	-681	26.000	60.000
SDOUT	-736.800	-681	26.000	60.000
D0	-836.800	-681	26.000	60.000
D1	-936.800	-681	26.000	60.000
D2	-1036.800	-681	26.000	60.000
D3	-1136.800	-681	26.000	60.000
D4	-1236.800	-681	26.000	60.000
D5	-1336.800	-681	26.000	60.000
D6	-1436.800	-681	26.000	60.000
D7	-1536.800	-681	26.000	60.000
E-($\overline{\text{RD}}$)	-1636.800	-681	26.000	60.000
R/ $\overline{\text{W}}$ -($\overline{\text{WR}}$)	-1736.800	-681	26.000	60.000
SD/ $\overline{\text{C}}$	-1836.800	-681	26.000	60.000
$\overline{\text{CS0}}$	-1936.800	-681	26.000	60.000
VDD_BG	-2036.800	-681	26.000	60.000
ROW0	-2111.500	-681	26.000	60.000
ROW1	-2175.500	-681	26.000	60.000
ROW2	-2239.500	-681	26.000	60.000
ROW3	-2303.500	-681	26.000	60.000
ROW4	-2367.500	-681	26.000	60.000
ROW5	-2431.500	-681	26.000	60.000
ROW6	-2495.500	-681	26.000	60.000
ROW7	-2559.500	-681	26.000	60.000
ROW8	-2623.500	-681	26.000	60.000
ROW9	-2687.500	-681	26.000	60.000
ROW10	-2751.500	-681	26.000	60.000
ROW11	-2815.500	-681	26.000	60.000
ROW12	-2879.500	-681	26.000	60.000

Table 4: Bottom Side (from right to left) (Sheet 4 of 4)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
ROW13	-2943.500	-681	26.000	60.000
ROW14	-3007.500	-681	26.000	60.000
ROW15	-3071.500	-681	26.000	60.000
ROW16	-3135.500	-681	26.000	60.000
ROW17	-3199.500	-681	26.000	60.000
ROW18	-3263.500	-681	26.000	60.000
ROW19	-3327.500	-681	26.000	60.000
ROW20	-3391.500	-681	26.000	60.000
ROW21	-3455.500	-681	26.000	60.000
ROW22	-3519.500	-681	26.000	60.000
ROW23	-3583.500	-681	26.000	60.000
ROW24	-3647.500	-681	26.000	60.000
ROW25	-3711.500	-681	26.000	60.000
ROW26	-3775.500	-681	26.000	60.000
ROW27	-3839.500	-681	26.000	60.000
ROW28	-3903.500	-681	26.000	60.000
ROW29	-3967.500	-681	26.000	60.000
ROW30	-4031.500	-681	26.000	60.000
ROW31	-4095.500	-681	26.000	60.000

Table 5: Left Side (from bottom to top)

Lead Pad Name	Pad Placements		Pad Dimensions	
	X	Y	X	Y
DUMMY_A8	-4245.300	-603.2	60.000	26.000
DUMMY_A7	-4245.300	-539.2	60.000	26.000
DUMMY_A6	-4245.300	-131.35	60.000	26.000
DUMMY_A5	-4245.300	-67.35	60.000	26.000
DUMMY_A4	-4245.300	-3.35	60.000	26.000
DUMMY_A3	-4245.300	60.65	60.000	26.000
DUMMY_A2	-4245.300	520	60.000	26.000
DUMMY_A1	-4245.300	600	60.000	26.000

1.4 Mechanical Dimensions

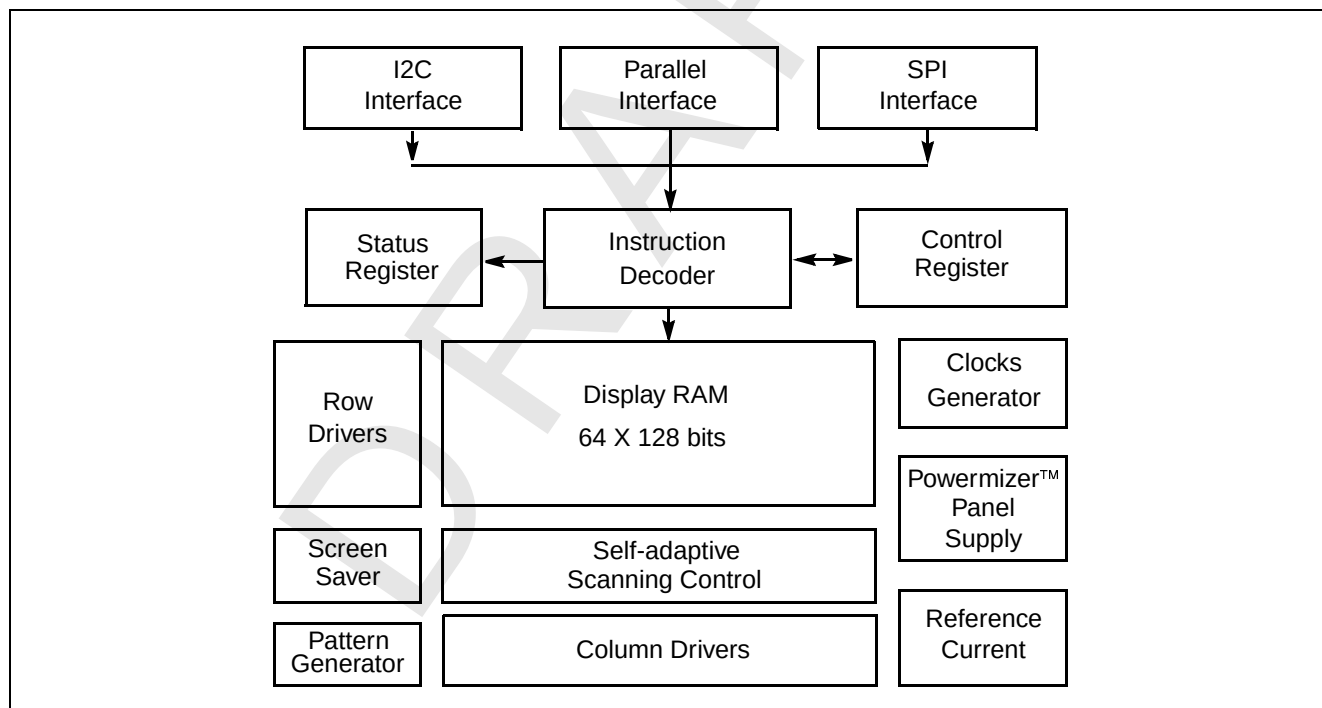
Table 6: Mechanical Dimensions

Description	Dimension
Die Size	8.73mm x 1.6mm
Pad Pitch	64µm (min.), 100µm (max)
Pad Size	26µm x 60µm
Wafer Thickness	450µm
Bump Size	40µm x 74µm x 20µm
Bump Characteristics	gold, electrolytic
Bump Hardness	30-80Hv

1.5 Functional Description

The architecture of the STV8102 provides all the functions to drive the OLED displays. The block diagram gives an overview of the different on-chip components and their links.

Figure 4: STV8102 Block Diagram



The description of the STV8102 functions is given in the following sections, starting with the bus interfaces.

2 Bus Interfaces

The STV8102 is always set in a slave configuration whatever the bus choice (the host is always providing the communication clock). For any kind of communication, the device has to be activated first by correctly positioning the chip select pins.

Table 7: Chip Select Pins

$\overline{\text{CS0}}$	Note
0	Communications enabled
1	Interfaces disabled and reset (device remains functional)

Moreover, each received data may be either a graphic data or a device instruction. That has to be indicated on the $\text{SD}/\overline{\text{C}}$ pin.

Table 8: Data/Instruction Selection

$\text{SD}/\overline{\text{C}}$	Note
0	Access to the registers (command &/or data)
1	Access to the display RAM (pixel data)

In I^2C mode, the $\text{SD}/\overline{\text{C}}$ pin must be kept at "0". To provide the widest flexibility and ease of use, the STV8102 features four different solutions for interfacing with the host controller. The SEL1 and SEL0 input pins select the appropriate interface as described in [Table 9](#).

Table 9: Interface Selection

SEL1	SEL0	Interface
0	0	I^2C (Standard or Fast)
0	1	Serial
1	0	Parallel (68xx)
1	1	Parallel (80xx)

Non-selected interfaces are reset.

The definitions and the specifications of the signals and timing diagrams given in the following sections provide functional information of the different interfaces.

2.1 I^2C Interface

The I^2C interface is compliant with the I^2C bus specification and able to work in both Standard (100kHz) and Fast Speed (400kHz) modes. The write address is 78h and the read address is 79h for the register access, and 7Ah for RAM write. (No RAM read available).

This bus is intended for communication between ICs. It consists of two lines: one bi-directional for data signals (SDA) and one input for clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via an active or passive pull-up.

During the communication, the $\overline{\text{SD/C}}$ pin must be kept grounded.

Figure 5: I²C Interface Timing Diagram for Register Write

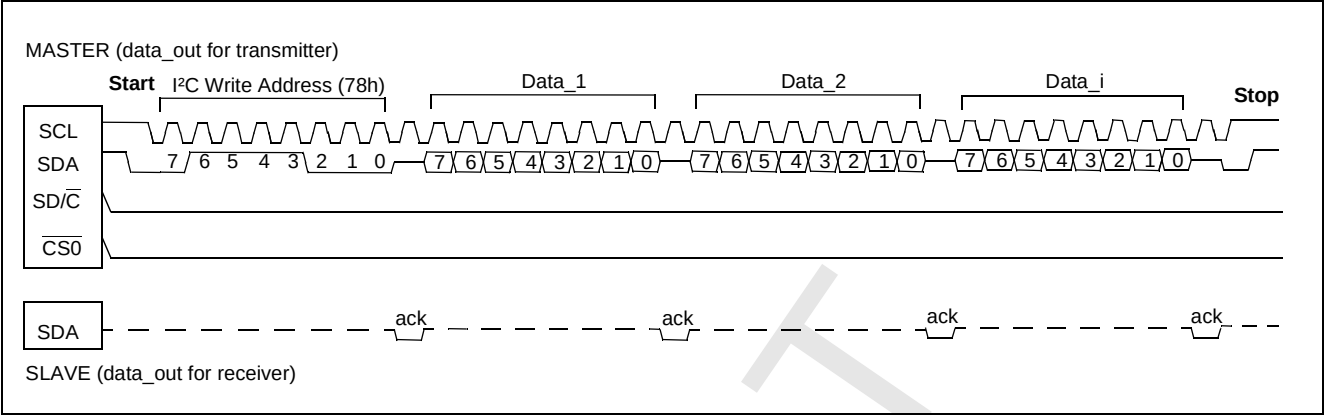


Figure 6: I²C Interface Timing Diagram for RAM Write

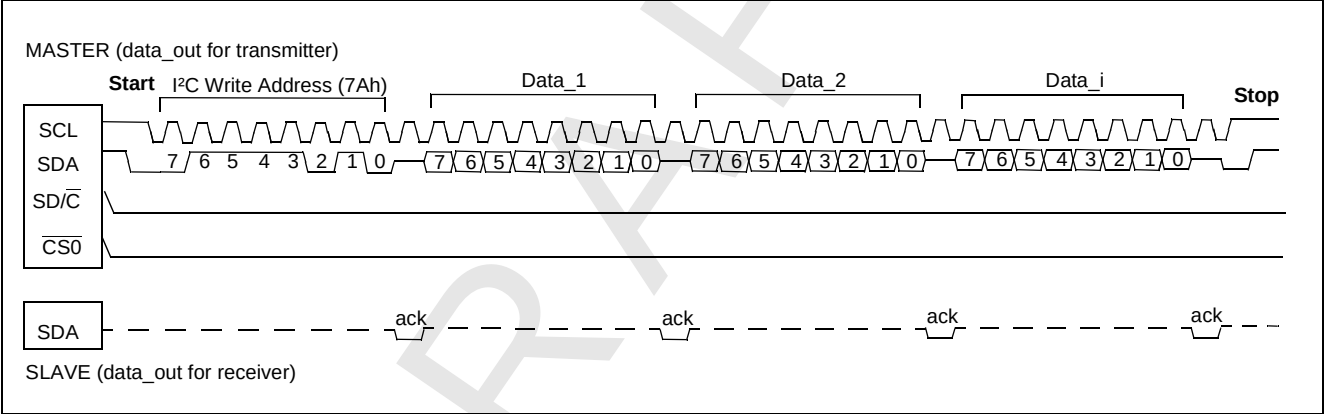


Table 10: I²C Interface Write Timing

Item	Description	Min.	Typ.	Max.	Unit
Tscl_cycle		2.5			μs
Tscl_low / Tscl_high		100/100			ns
Tscl_rise / Tscl_fall				15/15	ns
Tdatas / Tdatah	Data setup & hold	100/100			ns
Tcs0s / Tcs0h	Chip Select setup & hold	120/120			ns

Figure 7: I²C Interface Read Timing Diagram (Register only)

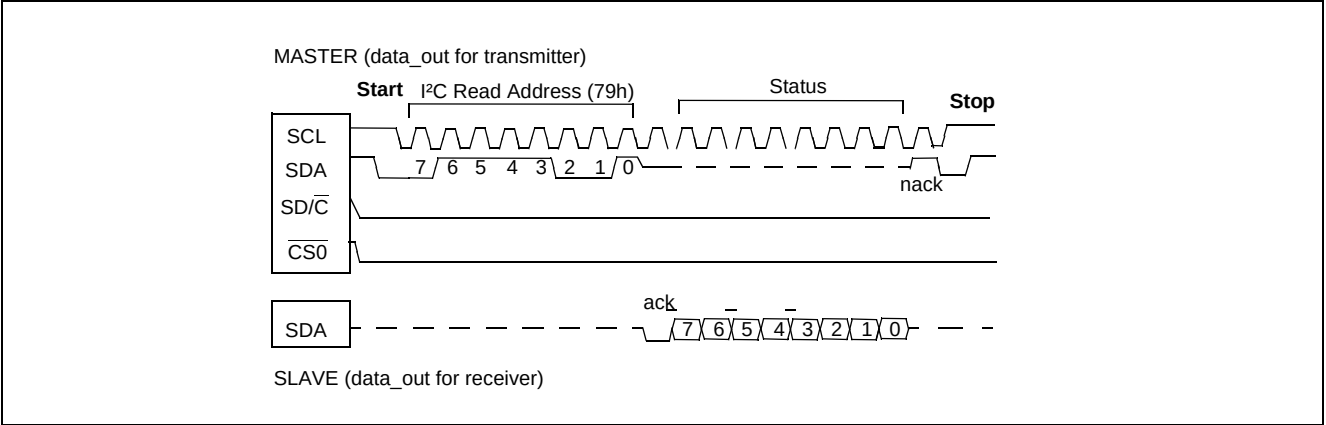


Table 11: I²C Interface Read Timing (Register only)

Item	Description	Min.	Typ.	Max.	Unit
Tscl_cycle		2.5			μs
Tscl_low / Tscl_high		100/100			ns
Tscl_rise / Tscl_fall				15/15	ns
Tdatas / Tdatah	Data setup & hold	100/100			ns
Tcs0s / Tcs0h	Chip Select setup & hold	120/120			ns

2.2 Serial Interface

The STV8102 serial interface is a bi-directional link between the display controller and the application supervisor. It consists of three lines: SDIN for data input, SDOUT for data output, SCLK for clock signal plus two control lines: $\overline{\text{CS0}}$ for chip select and $\overline{\text{SD/C}}$ for command or data selection. The SDIN and SDOUT pins can be connected together.

During data transfer, the data line is sampled on the positive SCLK edge shifting bits 8 per 8 starting from the chip selection.

Figure 8: Serial Peripheral Interface Timing Diagram (Write Mode)

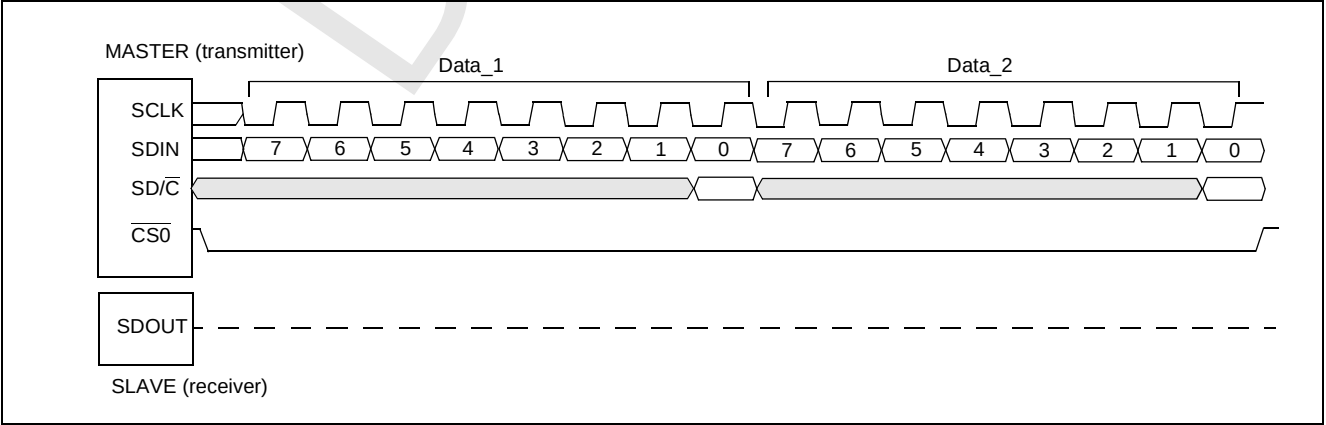


Figure 9: Serial Peripheral Interface Timing (Write Mode)

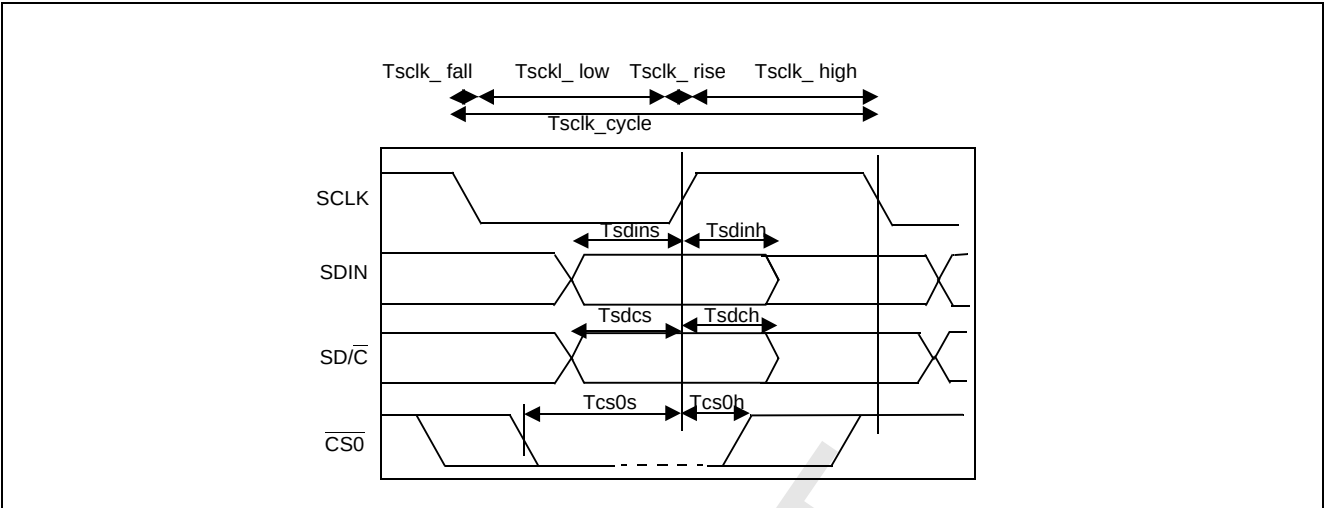


Table 12: Serial Peripheral Interface Timing (Write Mode)

Item	Description	Min.	Typ.	Max.	Unit
Tsclk_cycle		250			ns
Tsclk_low / Tsclk_high		100/100			ns
Tsclk_rise / Tsclk_fall				15/15	ns
Tsdins / Tsdinh	SDIN setup & hold	100/100			ns
Tsdcs / Tsdch	SD/C setup & hold	150/150			ns
Tcs0s / Tcs0h	Chip Select setup & hold	150/150			ns

Figure 10: Serial Peripheral Interface Timing Diagram for Register Read (only)

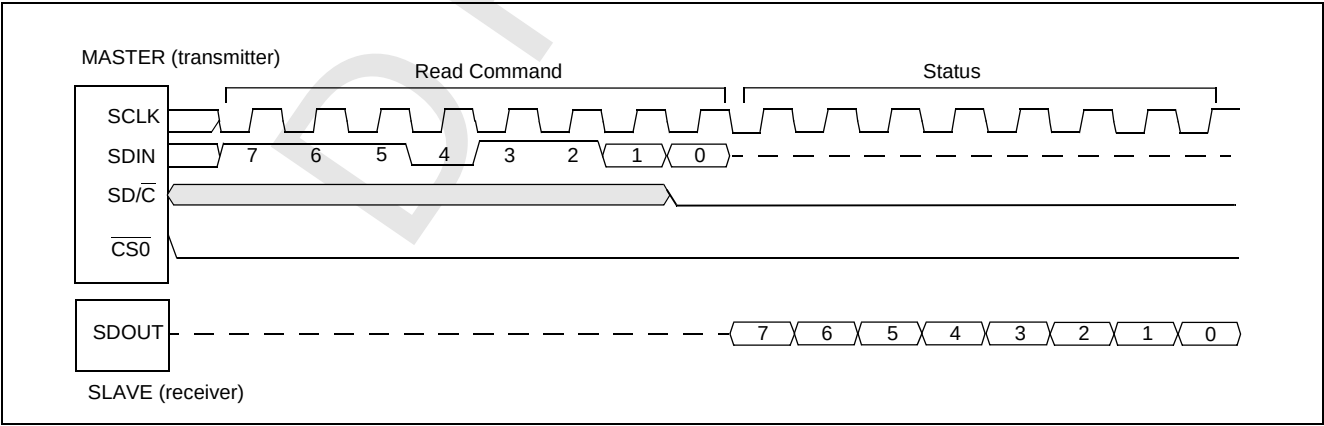


Figure 11: Serial Peripheral Interface Timing Diagram for Register Read (only)

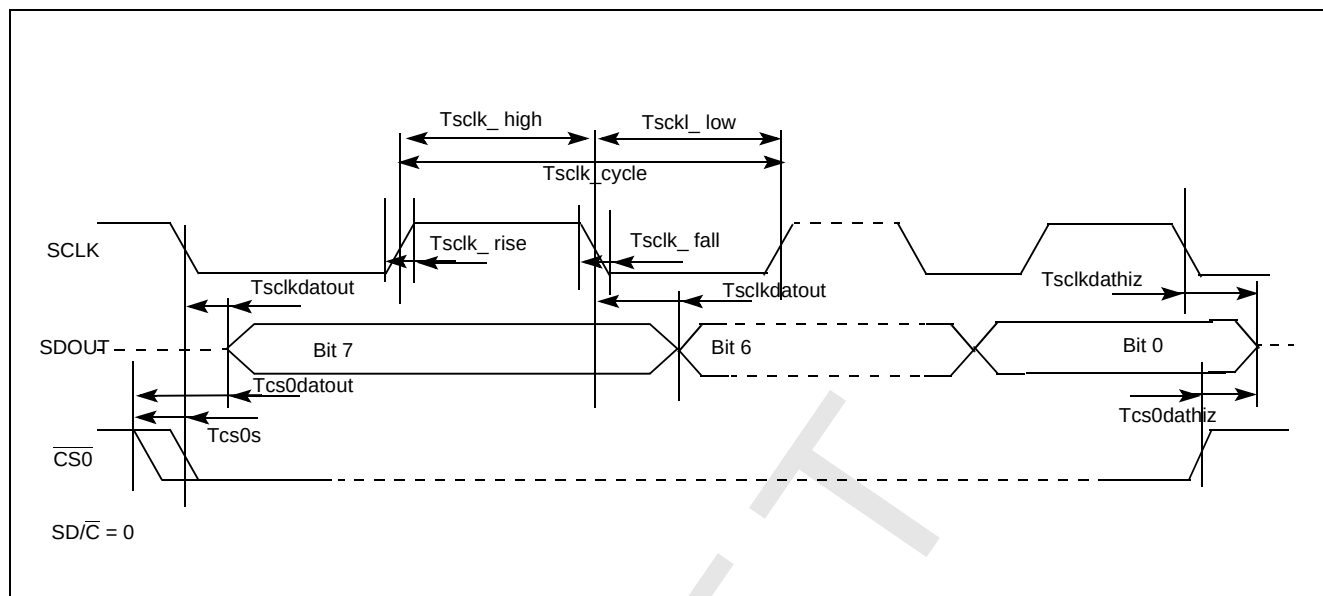


Table 13: Serial Peripheral Interface Timing Diagram for Register Read (only)

Item	Description	Min.	Typ.	Max.	Unit
Tscclk_cycle		250			ns
Tscclk_low / Tscclk_high		100/100			ns
Tscclk_rise / Tscclk_fall				15/15	ns
Tscclkdatout	Data output time after SCLK falling edge	TBD	50		ns
Tscclkathiz	Data output HiZ state time after SCLK falling edge	TBD	50		ns
Tcs0datout	Data output time after $\overline{CS0}$ falling edge	TBD	50		ns
Tcs0athiz	Data output HiZ state time after CS0 rising edge	TBD	50		ns
Tcs0s	Chip Select setup before SCLK rising edge	0			ns

2.3 Parallel Interface

The STV8102 parallel interface is a bi-directional link between the display driver and the application supervisor. It consists of twelve lines: eight data lines and four control lines: $\overline{E}$ -(RD), $\overline{R/W}$ -(WR), $\overline{SD/C}$ and $\overline{CS0}$. The control lines are used as for 68xx or 80xx series.

Figure 12: 8-Bit Parallel 68XX interface Timing Diagram (Write Mode)

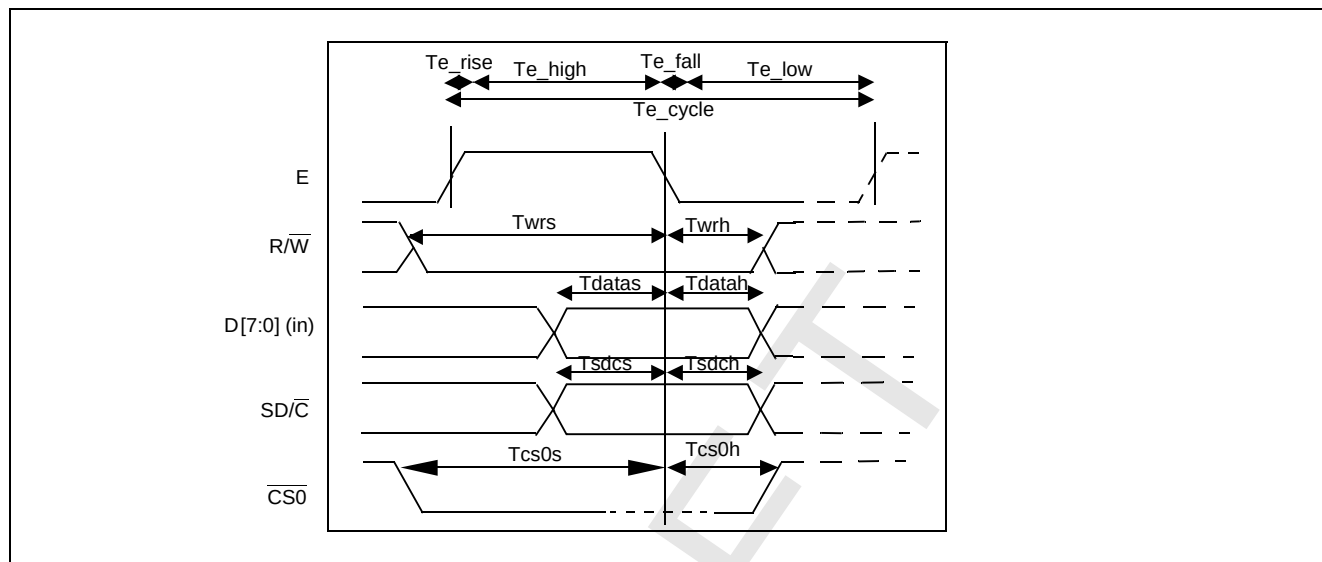


Table 14: 8-bit Parallel 68XX Interface Timing (Write Mode)

Item	Description	Min.	Typ.	Max.	Unit
Te_cycle		300			ns
Te_low / Te_high		60/60			ns
Te_rise / Te_fall				15/15	ns
Twrs / Twrh	$\overline{R/W}$ Write Data setup & hold	TBD	50/50		ns
Tdatas / Tdatah	Data Address setup & hold	25/25			ns
Tsdcs / Tsdch	$\overline{SD/C}$ setup & hold	TBD	60/60		ns
Tcs0s / Tcs0h	Chip Select setup & hold	TBD	120/60		ns

Figure 13: 8-Bit Parallel 68XX interface Timing Diagram for Register Read (only)

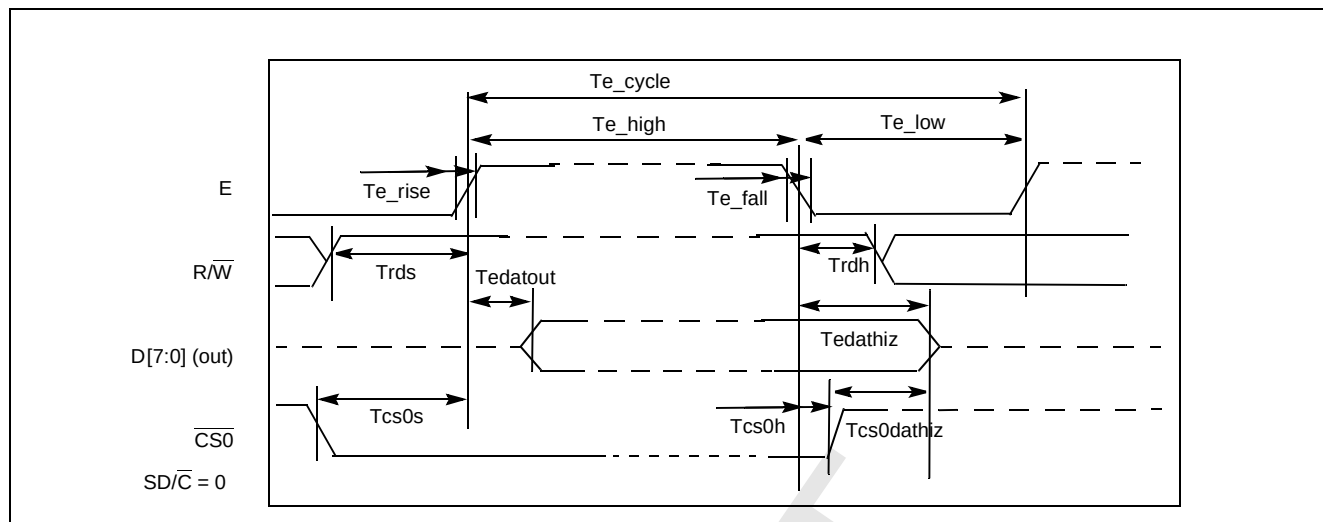


Table 15: 8-bit Parallel 68XX Interface Timing (Read Mode)

Item	Description	Min.	Typ.	Max.	Unit
Te_cycle		300			ns
Te_low / Te_high		120/60			ns
Te_rise / Te_fall				15/15	ns
Trds	READ setup to E rising edge (with CL = 100pF)	TBD	50		ns
Trdh	READ hold from E falling edge (with CL = 100pF)	TBD	50		ns
Tedatout	Data out from E rising edge	-	20	TBD	ns
Tedathiz	Data Hiz from E falling edge	-		TBD	ns
Tcs0dathiz	Data Hiz from $\overline{\text{CS0}}$ rising edge	-		TBD	ns
Tcs0s / Tcs0h	Chip Select setup & hold	120/60			ns

Figure 14: 8-bit Parallel 80XX Interface Timing Diagram (Write Mode)

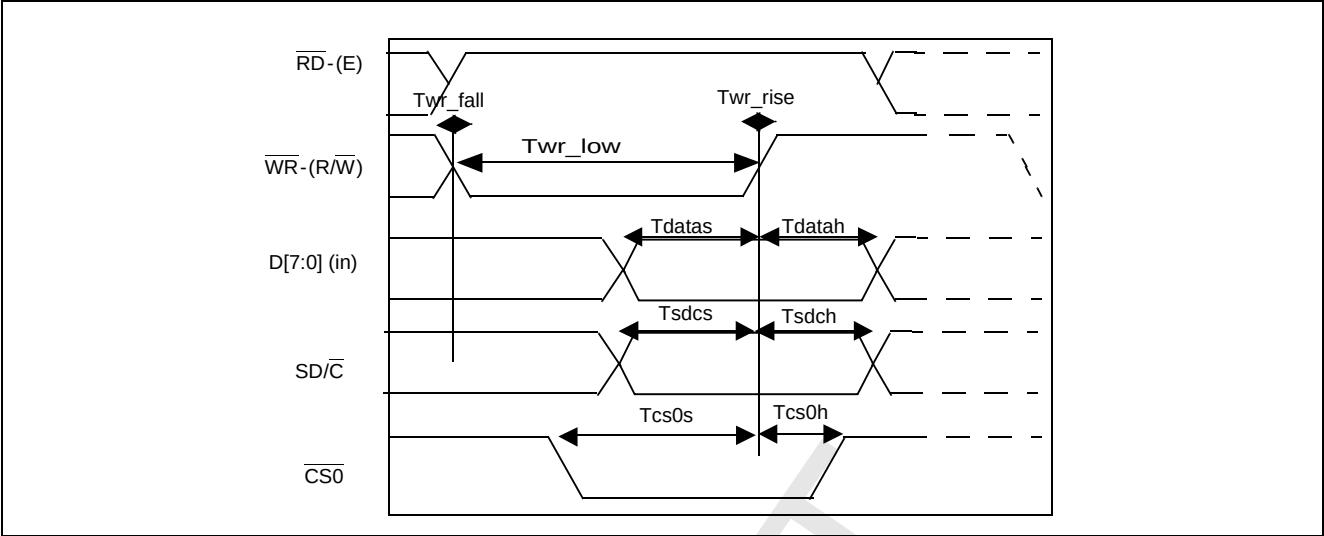


Table 16: 8-bit Parallel 80XX Interface Timing (Write Mode)

Item	Description	Min.	Typ.	Max.	Unit
Twr_low		60			ns
Twr_rise / Twr_fall				15/15	ns
$Tdatas / Tdatah$	Data Address setup & hold	25/25			ns
$Tsdcs / Tsdch$	$\overline{SD}/\overline{C}$ setup & hold	TBD	60/60		ns
$Tcs0s / Tcs0h$	Chip Select setup & hold	TBD	120/60		ns

Figure 15: 8-bit Parallel 80XX Interface Timing Diagram (Read Mode)

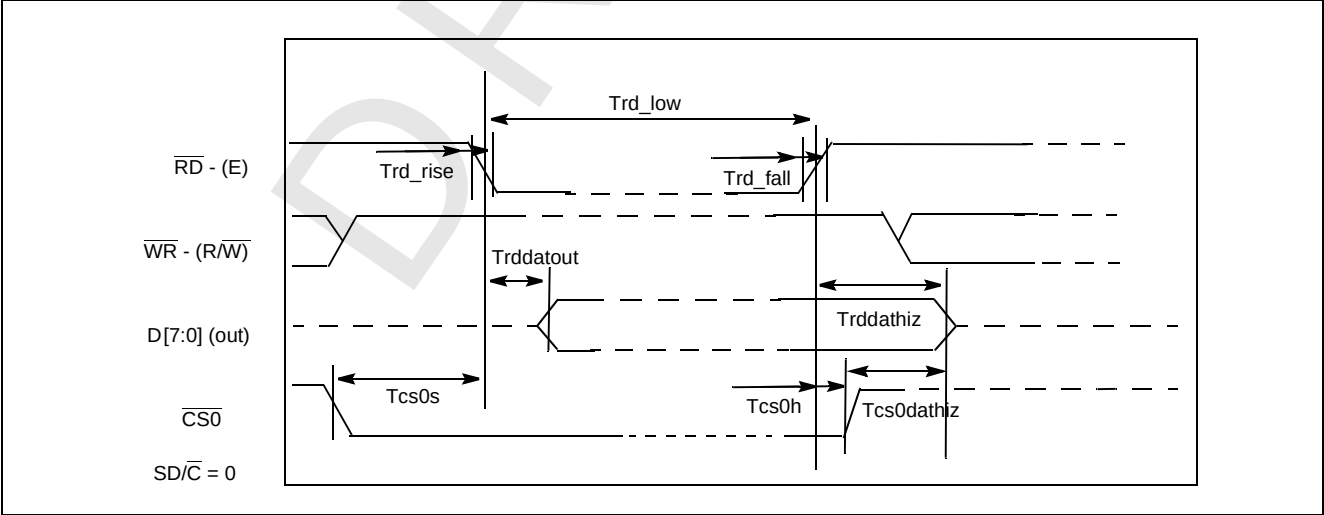


Table 17: 8-bit Parallel 80XX Interface Timing (Read Mode)

Item	Description	Min.	Typ.	Max.	Unit
Trd_low		120			ns
Trd_rise / Trd_fall				15/15	ns
Trddatout	Data out from $\overline{RD}$ falling edge (with CL = 100pF)		20	TBD	ns
Trddathiz	Data Hiz from $\overline{RD}$ rising edge (with CL = 100pF)			TBD	ns
Tcs0dathiz	Data Hiz from $\overline{CS0}$ rising edge			TBD	
Tcs0s / Tcs0h	Chip Select setup & hold	120/60			ns

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3 Display RAM

The RAM of the STV8102 stores data to be displayed on the OLED matrix in a format of one bit per pixel. If the bit value is a logical “1”, the corresponding pixel is ON; if “0” the pixel is OFF. The RAM organization is always seen by the user as a set of sixty-four rows (Y0 to Y63) of sixteen bytes (X0 to X15) as described in [Figure 16](#). There are several ways to display the bits of the RAM on the pixels of the screen. These ways are detailed in [Chapter 4: Display Modes](#). As the pixel location depends on the application and the hardware mapping of the display, the bit/pixel selection is mainly done during start-up. For more information, refer to [Chapter 4: Display Modes](#) and [Chapter 9: STV8102 Configuration](#).

RAM loading is done through the selected interface in 8-bit format. The RAM access mode is sequential with the possibility to select the starting location. A row mode is provided for fast loading and clearing.

Figure 16: Display RAM Organization

BYTE	X0	X1	- - -	X13	X14	X15
Row Y0	b0---b7	b0---b7	- - -	b0---b7	b0---b7	b0---b7
Row Y1			- - -			
Row Y2			- - -			
- - -	- - - - - - - - - - - - - - - -					
Row Y62			- - -			
Row Y63			- - -			

3.1 RAM Writing

The RAM organization is a set of in sixty-four rows (Y0 to Y63) of sixteen bytes (X0 to X15) as described in [Figure 16](#).

Writing to a RAM location starts at the address defined by the XSTART (0 to 15) and YSTART (0 to 63) registers. On a hardware reset, the registers are cleared, so any write to the RAM starts at location (X0, Y0). To be loaded as RAM data, pin SD/C must be held high during the interface transfer, otherwise the data is decoded as a command or a register setting. By default (PIXLMAP register), bytes are loaded into RAM with the most significant bit the first received in serial mode and/or with the most significant as bit 7 in parallel mode (See Control and Status Register Description chapter for detail).

The XSTART & YSTART registers are automatically incremented after each byte write, so writes can be automatically done from X0 and Y0,... up to X15 & Y63 and back to X0 & Y0. Without any update of XSTART & YSTART registers, continued RAM access restarts at the last accessed location (+1). Any RAM location can be loaded by programming the XSTART & YSTART registers with the right value.

Updating the RAM can be done in Row Access mode using the RAMROW command. (For more information, refer to [Chapter 10: Control and Status Registers Description](#).) In this mode, the write starts at the row defined by the current YSTART register. All the 16 bytes of the row (X0 to X15) are loaded with the same byte data. The YSTART register is automatically incremented at each written data. For example, it takes 64 writes of data “00h” to clear the entire RAM in Row Access mode.

4 Display Modes

The STV8102 can be connected to the display electrodes with different configurations to drive most of the OLED matrixes. A set of configuration registers brings the flexibility required by the different system architectures. These capabilities are described in more detail in [Chapter 9: STV8102 Configuration](#).

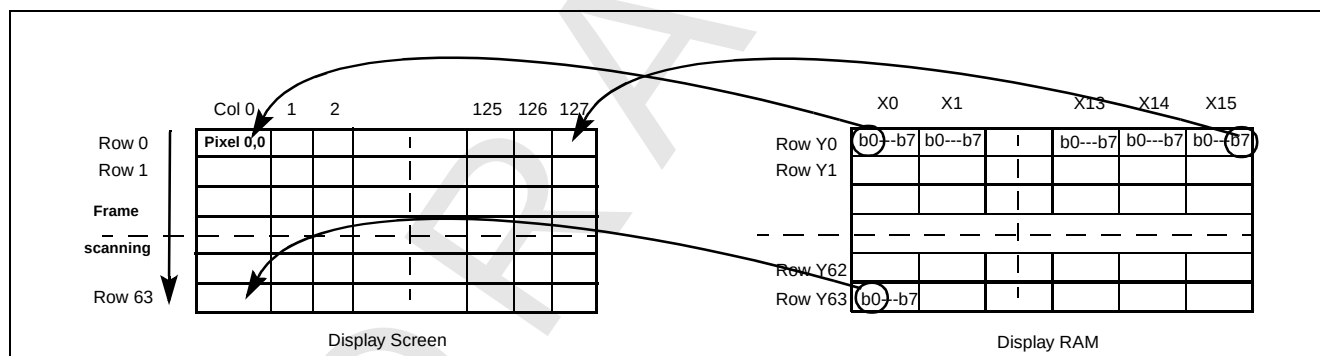
In the following sections, it is assumed that the hardware display configuration leads to display pixel 0,0 at the top-left side of the display when registers and commands are set to “Normal Horizontal/Vertical display” and when the data RAM is loaded from X0-Y0 to X15-Y63 with the most significant bit first. Note that the row and column display counters are independent of the Xn-Yn RAM access counters and are not user-accessible.

4.1 Normal Horizontal/Vertical Display

This is the default mode after power-up and reset of the controller taking into account the above mentioned assumptions. The STV8102 starts to display pixel 0,0 at the top-left side of the screen reading bit 0 of RAM location X0-Y0 (refer to [Figure 17](#)). The complete row (X0 to X15) is loaded in the column drivers and the row display counter is automatically incremented and so on up to the last pixel 127,63 read at RAM location X15-Y63.

Row and column display counters restart at location X0-Y0 at each frame. The column drivers are loaded with RAM data. Frame scanning starts from the top to the bottom of the screen.

Figure 17: Normal Horizontal-Vertical Mode



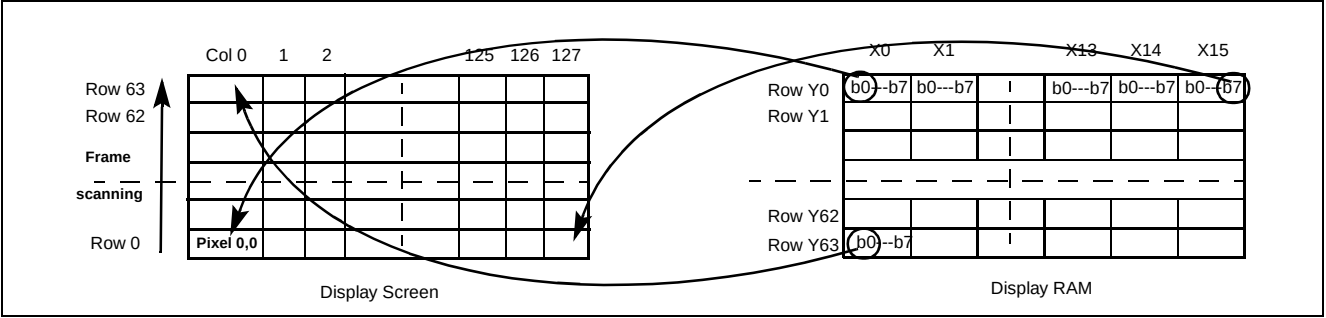
4.2 Mirrored Modes

4.2.1 Mirrored Vertical

In this mode, the first pixel of the frame is displayed at the bottom-left side of the screen loading bit 0 of X0-Y0 location up to bit 127 of X15-Y0 in the column drivers (refer to [Figure 18](#)).

The row display counter is automatically decremented down to row 0 (corresponding to RAM row Y63) and restarts at row 63 (RAM row Y0) at each frame. Frame scanning starts from the bottom to the top of the screen.

Figure 18: Vertical Mirrored Mode

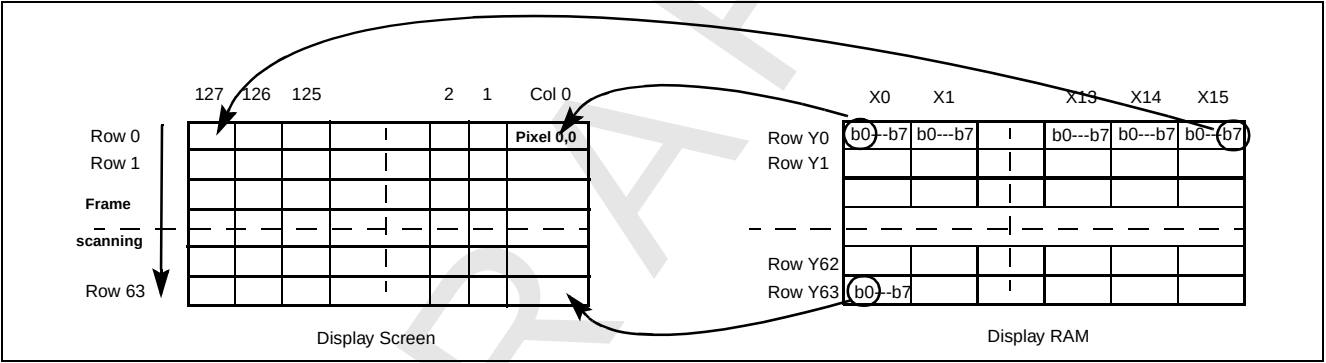


4.2.2 Mirrored Horizontal

Using this mode the first pixel of the frame is displayed at the top-right side of the screen loading bit 0 of location X0-Y0 up to bit 127 of location X15-Y0 in the column drivers (refer to [Figure 19](#)).

The display of the row is the reverse order of the bits of RAM locations X0/X15-Yn. Frame scanning starts from the top to the bottom of the screen.

Figure 19: Horizontal Mirrored Mode



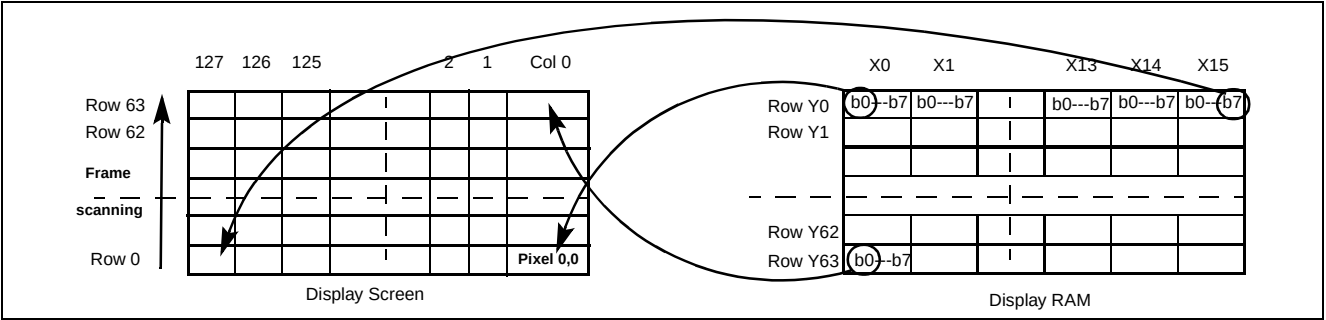
4.2.3 Full Mirror

This mode is the combination of Horizontal and Vertical Mirrored modes.

The first pixel of the frame is displayed at the bottom-right side of the screen loading bit 0 of location X0-Y0 up to bit 127 of location X15-Y0 in the column drivers (refer to [Figure 20](#)).

Frame scanning starts from the bottom to the top of the screen.

Figure 20: Full Mirrored Mode



4.3 Display Panning

The STV8102 provides a panning mode to shift the display in a selected direction for a given number of pixels. The panning is a static function. The horizontal shift is controlled with the HSHIFT command followed by a signed byte giving the shift value in pixel units (from -128 to +127).

The vertical shift is controlled with the VSHIFT command followed by a signed byte giving the shift value in row unit (from -64 to +63).

After a hardware reset, HSHIFT and VSHIFT are set to 0 (their default value), the display perfectly fits the screen, and all pixels are displayed.

Remark: Display Panning and Screen Saver functions are disabled when “divide-by-4” of the reference clock is selected, that is when DIV.OSCCTRL is Set. Refer to [Table 20: List of Registers](#).

The description of the panning behavior is based on assumptions mentioned for the “Normal Horizontal/Vertical display” mode. It can be used with a Mirrored mode.

Vertical and horizontal shifts can be combined. Display examples are given in [Figure 21](#) and [Figure 22](#).

The Display RAM contents are not modified by the panning mode.

The “external” pixels of a shifted image can be blanked (default mode) or displayed in the folded area (wrapping mode). The wrapping mode is selected by the dedicated MOVE.HMOVE and/or MOVE.VMOVE bitfields. (For more information, refer to [Section 10: Control and Status Registers Description](#).)

Figure 21: Display Panning Mode (without Wrapping)

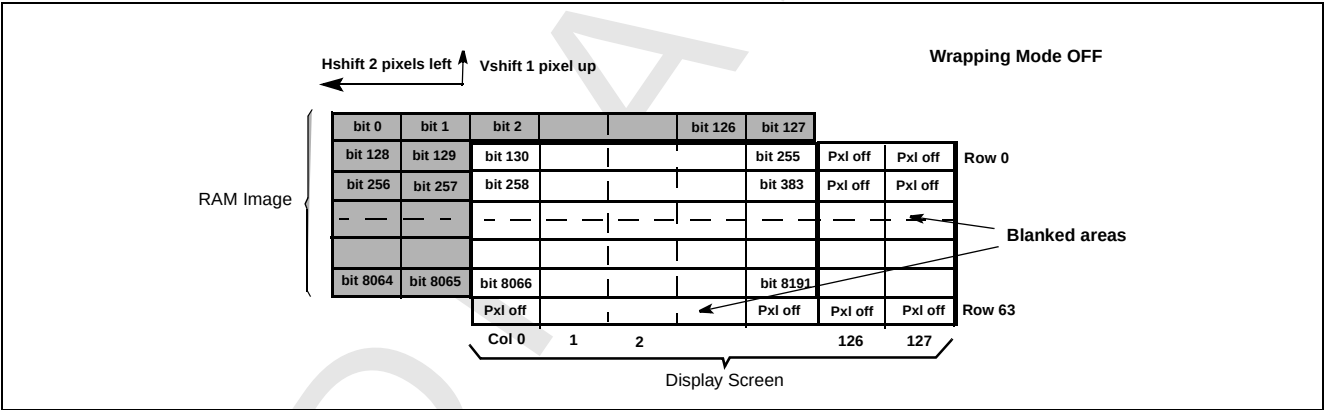
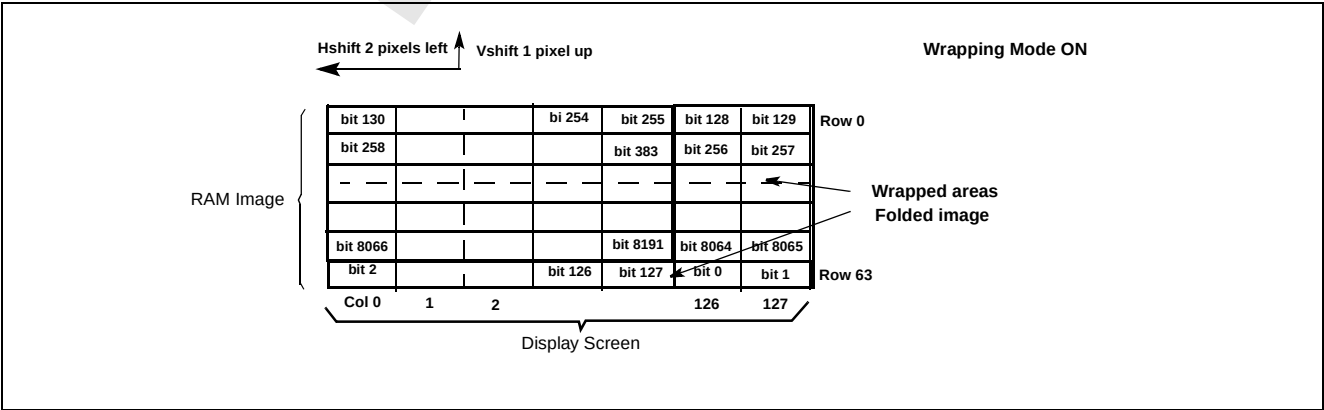


Figure 22: Display Panning Mode (with Wrapping)



4.4 Screen Saver

The STV8102 provides an automatic means for uniform pixel aging-compensation during periods when the system is not operated. The STV8102 stand-alone screen saver saves the host processor from having to provide the image and load it into the RAM. Once initialized, the screen saver operates “stand-alone”.

The description of the screen saver behavior is based on the assumptions mentioned for the “Normal Horizontal/Vertical display” mode. It can be used with a Mirrored mode.

The Pattern Generator function cannot be activated when the screen saver is operating.

The screen saver is an improvement of the panning function described previously. The shift of the image is done gradually, frame after frame, by selecting the speed of the motion with the HSPEED and/or VSPEED registers.

The horizontal speed can be 1 pixel per 1, 2 or 3 frames. The vertical speed can be 1 row per 1, 2 or 3 frames.

The HSHIFT and VSHIFT registers are incremented at each frame with one selected unit of speed. Their starting default values are 0. If the HSHIFT and VSHIFT values are different from 0, the start of the motion begins with a jump to the position defined by HSHIFT and VSHIFT.

The start of the motion is selectable for top/bottom and left/right directions using the VSPEED and HSPEED commands, respectively.

When started, the STV8102 automatically controls the motion of the picture within the limits set in the boundary registers.

The horizontal limits are set in HMIN and HMAX registers with a range of -128 to +127 pixels.

Vertically, registers VMIN and VMAX cover a range of -64 to +63 rows.

Different display effects can be selected when the picture reaches one of these limits (HSHIFT and/or VSHIFT registers value equals HMIN/HMAX and/or VMIN/VMAX).

To simplify the description of the cases, let us assume that only the horizontal motion is activated.

The same description applies to the vertical direction with the corresponding registers and both directions can be activated at the same time.

Remark: Display Panning and Screen Saver functions are disabled when “divide-by-4” of the reference clock is selected, that is when DIV.OSCCTRL is Set. Refer to [Table 20: List of Registers](#).

Example 1

Consider the motion of display row 0 only, with a full RAM display data row (X0 to X15 loaded with active pixels) HSHIFT is 0, HMAX is +100, HMIN is +32 and HSPEED is 1 pixel per frame to the right. HSHIFT is incremented frame after frame up to HMAX (+100).

Example 2

The conditions are the same as the first example, but the limits are set to the minimum/maximum with HMIN at -128 and HMAX +127.

In case of inconsistency between the starting positions and the limit settings, the logic of the controller forces the image within the limits. In the first example, at the first frame, the pixel 0,0 of the picture is moved from position 0,0 to position 32,0 of the screen and HSHIFT is loaded with HMIN (+32), in the second example the pixel 0,0 stays in position 0,0 and starts to move from this position because it is within the horizontal limits.

4.4.1 Limit-to-Limit

If the “**Limit-to-Limit**” effect (which is without wrapping) is selected using HMOVE register, the entire row shift to the right and when HSHIFT reaches HMAX, HSHIFT is loaded with HMIN and the picture row jumps back to the corresponding position (pixel 0,0 in position 32,0) as shown in Example 1. The motion restarts to the right. The pixels of the screen on the left of pixel 0,0 of the picture are blanked from the start of the motion (see [Figure 23](#) and [Figure 24](#)).

Figure 23: Limit to Limit Effect - Example 1 (Without Wrapping)

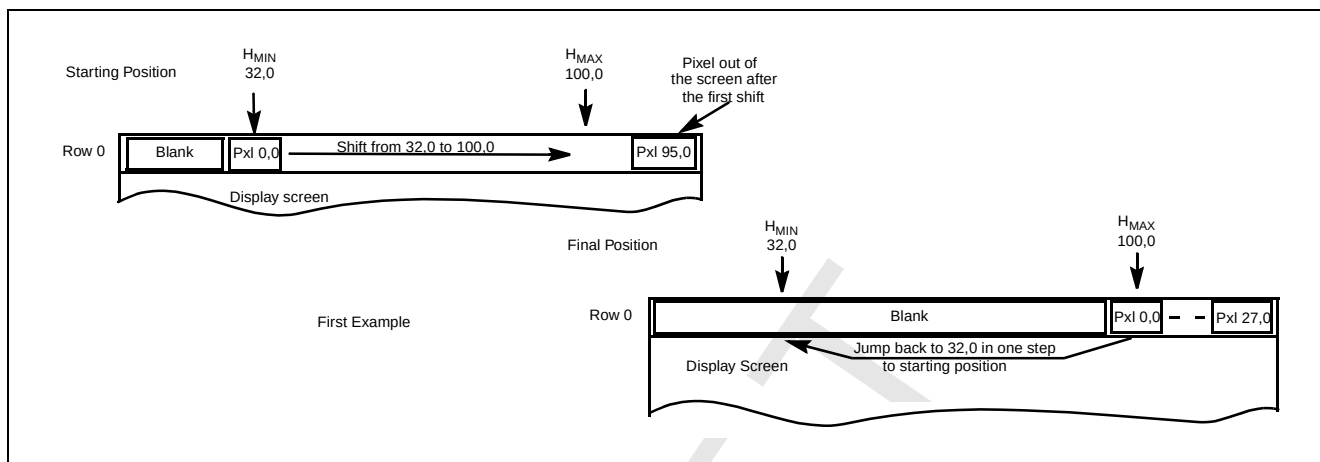
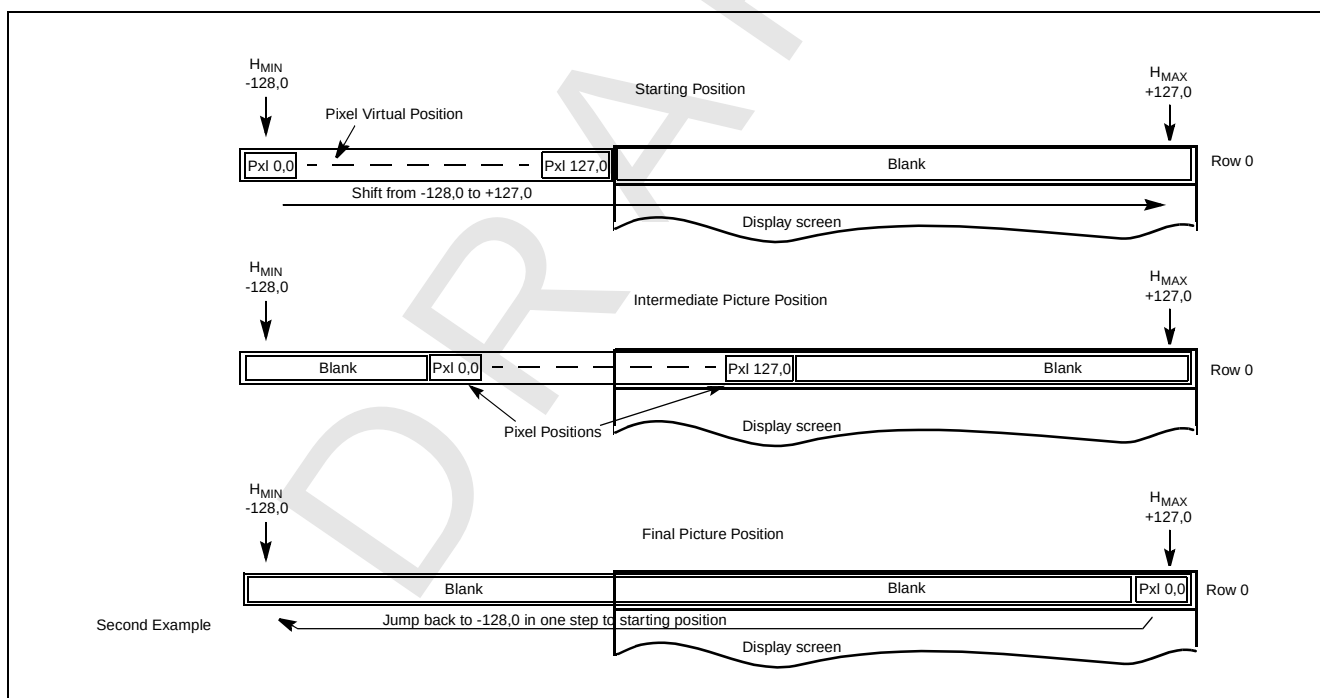


Figure 24: Limit-to-Limit Effect - Example 2 (without Wrapping)



4.4.2 Bounce Only

If the “**Bounce Only**” effect is selected, the entire row shift to the right starting from position 32,0 (as shown in Example 1) and when HSHIFT reaches HMAX, HSHIFT is decremented up to HMIN and so on. All the pixels of the screen on the left of pixel 0,0 of the picture are blanked. Only the right side of the row is displayed (see [Figure 25](#) and [Figure 26](#)).

Figure 25: Bounce Only - Example 1

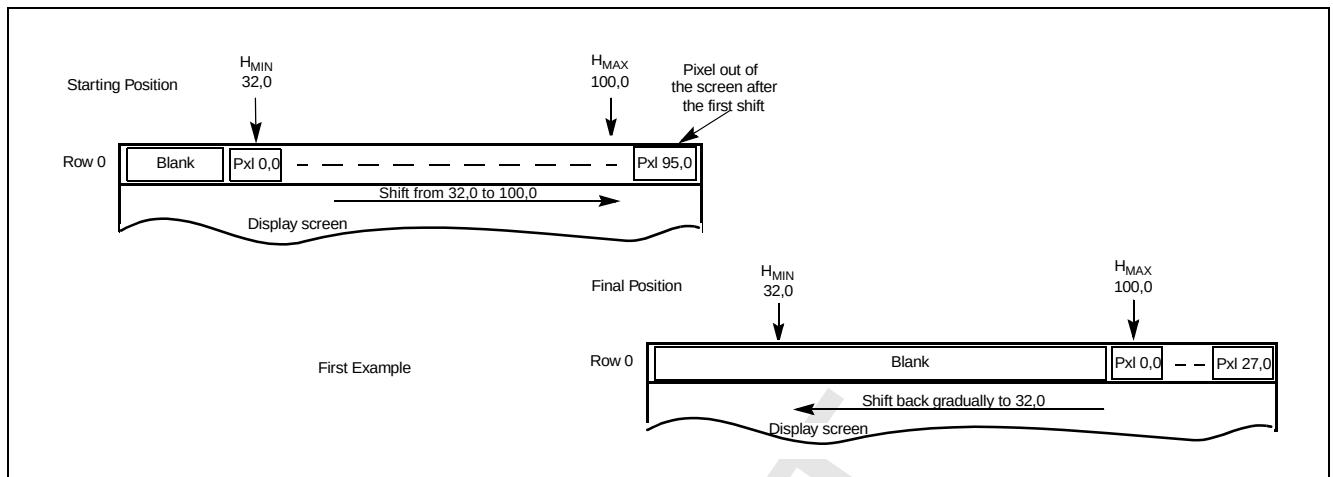
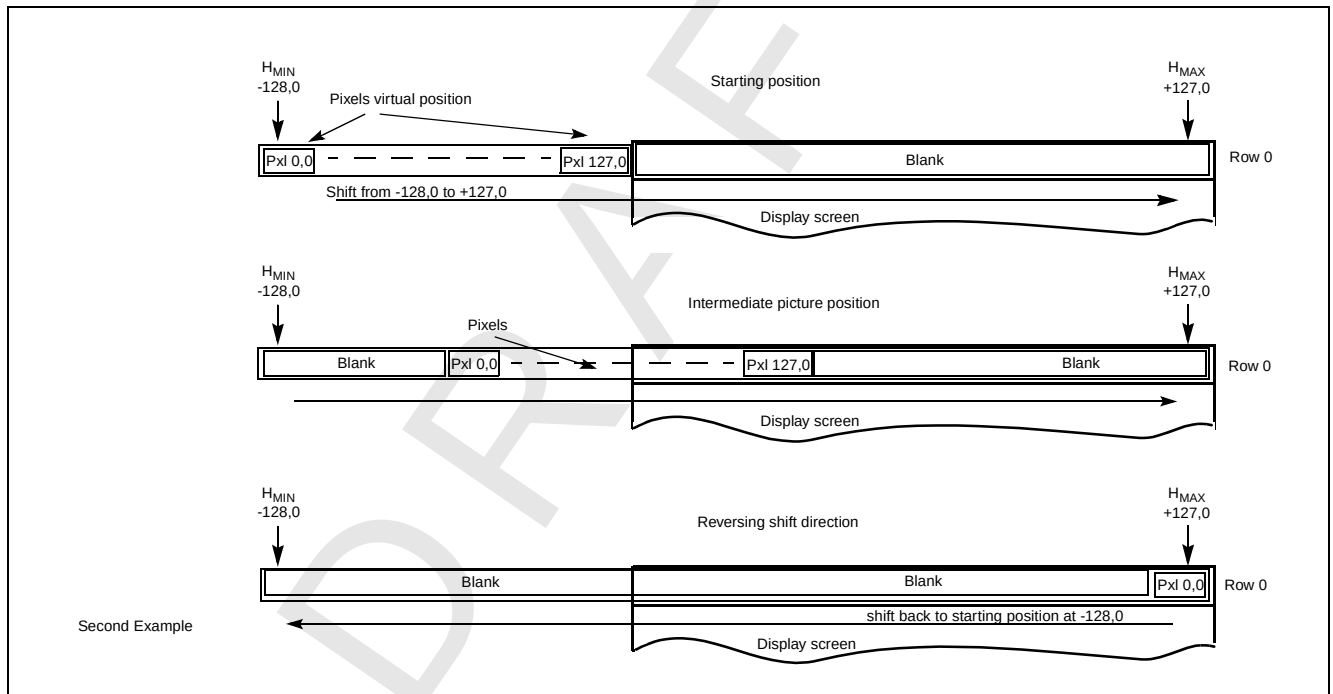


Figure 26: Bounce Only - Example 2



4.4.3 Wrap Only

If the **“Wrap Only”** effect is selected, the display effect is the same as the previous one, but all pixels of the row are displayed in a folded way (pixel 127,0 and pixel 0,0 remain consecutive and there are no blank pixels (see [Figure 27](#) and [Figure 28](#))).

Figure 27: Wrap Only - Example 1

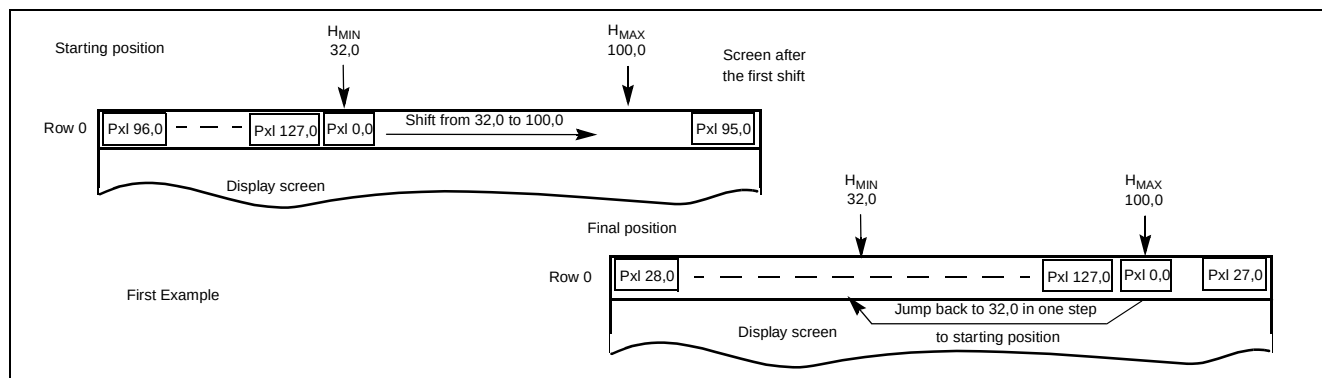
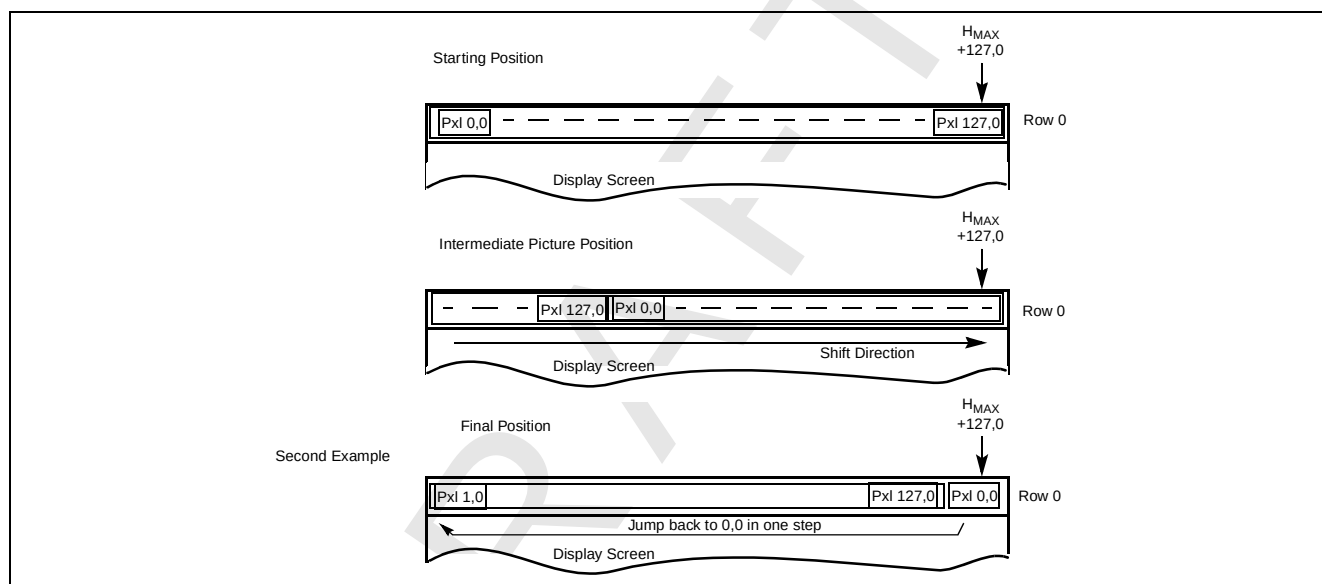


Figure 28: Wrap Only - Example 2



4.4.4 Wrap and Bounce

Selecting the “**Wrap and Bounce**” effect brings the same display effect as Bounce Only, except that all pixels of the picture are displayed in a folded way instead of being blanked (see [Figure 29](#) and [Figure 30](#)).

Figure 29: Wrap and Bounce - Example 1

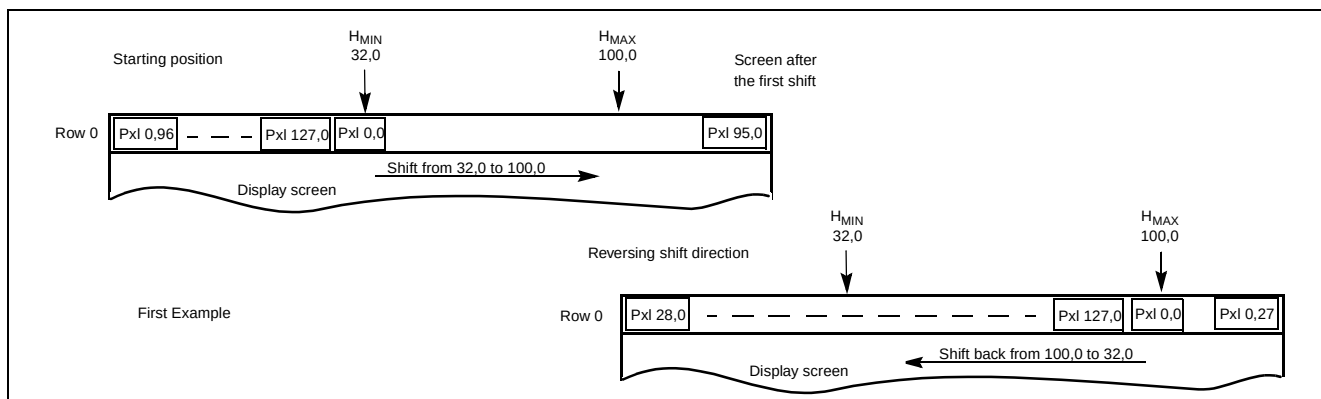
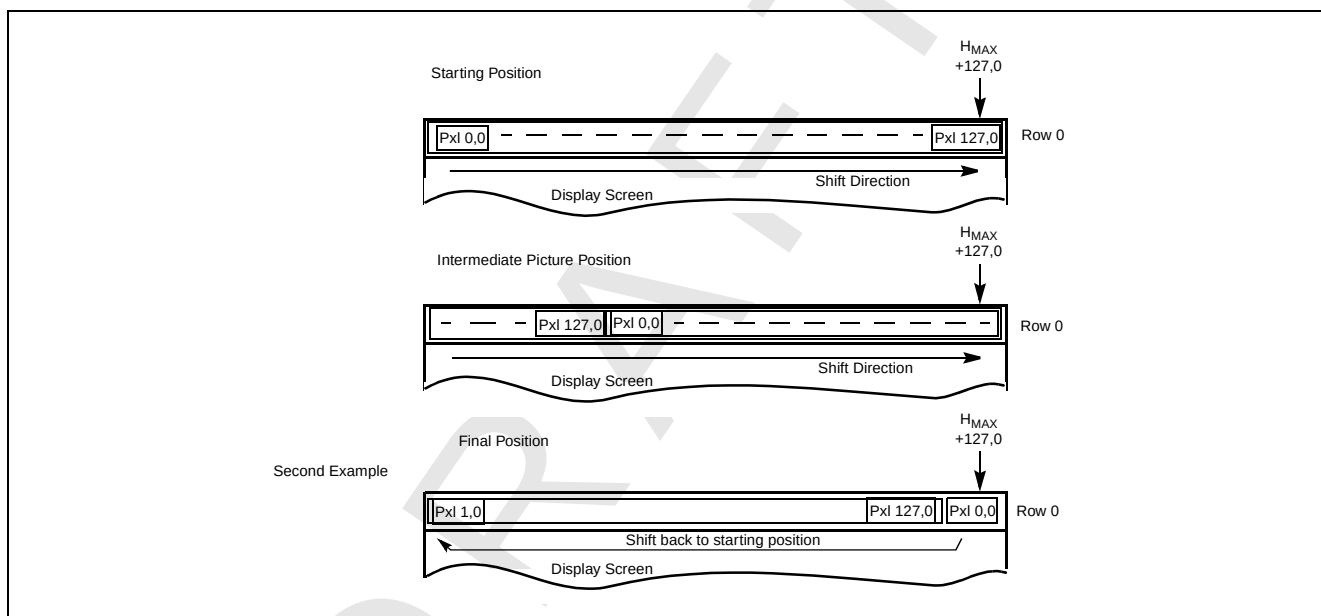


Figure 30: Wrap and Bounce - Example 2



In "Screen Saver mode", the brightness control and the scanning control are still operating. It is recommended to limit the number of active lines to minimize power consumption while the system is not operating. It is also recommended to set display brightness to a low value to optimize power consumption during screen saving operations.

4.5 Flash Mode

The STV8102 supports two Flash modes. In both case the Host has to send a dedicated command.

The first is to control the display with the Display ON/OFF instruction; this mode drastically reduces power dissipation. For more information, refer to [Chapter 6: Scanning Control](#) and [Chapter 11: Electrical Characteristics](#).

The second way uses the passive mode of the SCANMODE command and the RAMSCAN control register by selecting all row blocks OFF and ON at the flashing frequency. For more information, refer to [Chapter 6: Scanning Control](#) and [Chapter 10: Control and Status Registers Description](#).

4.6 Pattern Generator

The pattern generator block has been designed to help debugging of the application and simplify the panel pre-aging process during production.

Pattern generation is activated by sending the PATTERN_EN command. (Activated by sending D7h, de-activated by sending D6h.)

The pattern is selected with bits 0, 1 and 2 of the PATTERN_SEL command.

The displayed pattern is not written in the data RAM. The 'Display Control' block directly drives the row and column drivers with the appropriate control signals. Each pattern is a full screen picture of 128 x 64. The pattern mode has priority over all other selected display modes.

The 8 patterns implemented in the STV8102 are listed in [Table 18](#).

The activation of the PATTERN_ON input pin (from "0" to "1") resets the selection to the 1st pattern of the table. The different patterns are accessed sequentially by the mean of the pulses applied on the PATTERN_SELECT pin. After 8 pulses, the 1st pattern is activated again.

Table 18: Display Pattern Selection

b2 b1 b0	Description
0 0 0	All columns, all rows with blanked pixels (black screen)
0 0 1	All rows with black-white pixels (black and white columns)
0 1 0	Odd rows with black-white pixels, even rows with white-black pixels (Checker board)
0 1 1	Odd rows with all white pixels, even rows with all black pixels (white and black rows)
1 0 0	Odd rows with all black pixels, even rows with all white pixels (black and white rows) (complement of pattern 4)
1 0 1	All rows with white-black pixels (white and black columns, complement of pattern 2)
1 1 0	Odd rows with white-black pixels, Even rows with black-white pixels (complement of pattern 3)
1 1 1	All columns, all rows with on pixels (white screen) (complement of pattern 1)

5 Display Addressing Scheme

LEP/OLED panels are matrix displays driven in a progressive way. Lines 1 to N of the panel are selected successively during the row period while the data information is applied on the column electrodes. The active pixels are defined by the intersection of the selected line and the column electrodes.

Prior to the latching of the data information on the column electrodes, a dedicated sequence is applied on both row and column electrodes of the panel as described in the following sections.

5.1 Row Driver

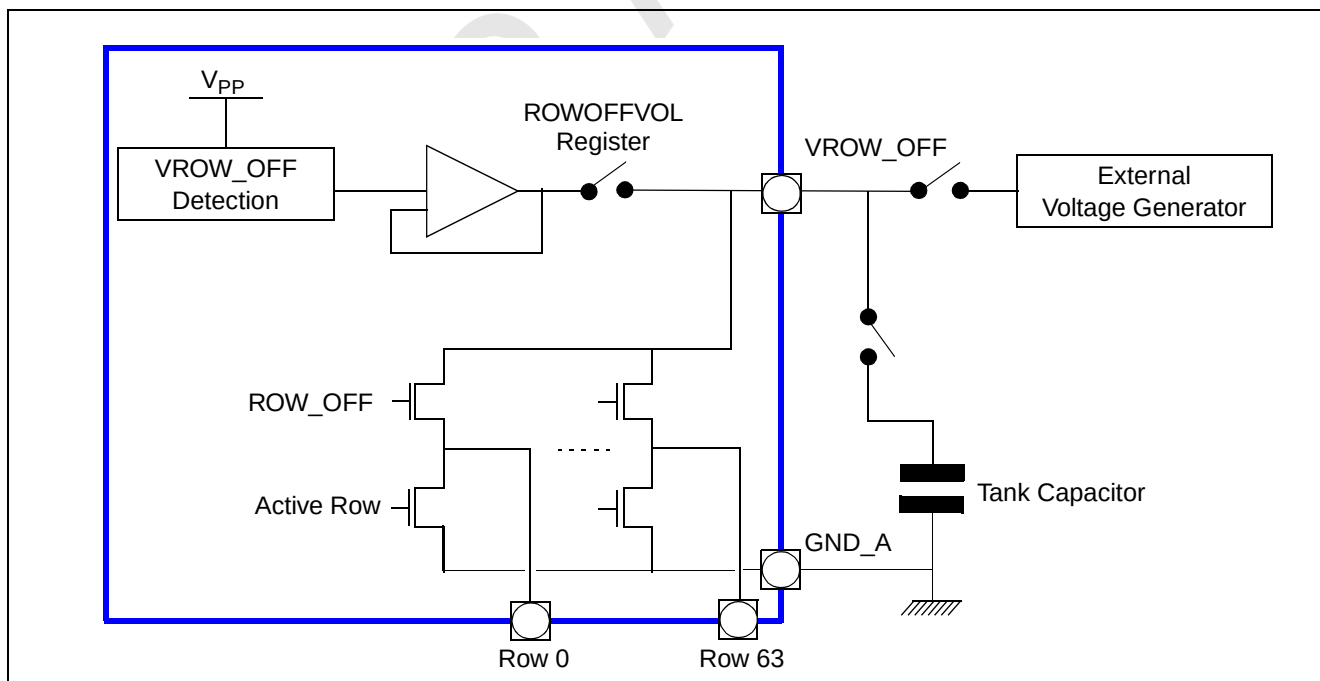
The elementary row driver output stage consists of a N-channel DMOS that sinks the various column currents collected in the row electrode during the “on” (active) period and a PMOS that switches the off rows to the $V_{\text{ROW_OFF}}$ off-state voltage.

To address the OLED display, the selected row is switched at low level (on state), the (N-1) rows of the circuit are switched at high level (off state). The $V_{\text{ROW_OFF}}$ off-state voltage can be selected as:

- an internal voltage adjusted automatically to the brightness level and the pixel operating voltages,
- an external voltage connected to pins $V_{\text{ROW_OFF}}$. It is important to note that $V_{\text{ROW_OFF}}$ must be lower than V_{PP}
- a tank capacitor connected to pins $V_{\text{ROW_OFF}}$ in order to collect capacitive current losses and to provide a row off state voltage close to the OLED threshold voltage.

The 3 off state voltages are selected by register ROWOFFVOL.

Figure 31: Row Driver Voltage Diagram



To reduce power consumption, the R_{ON} of the sink DMOS transistor is low. (For more information, refer to [Chapter 11: Electrical Characteristics](#).)

An optional, High Impedance mode (register ROWHIZ) can be used when no row off voltage is applied.

5.2 Column Driver

The elementary column driver output stage consists in a current mirror that sources brightness current in the column electrode of the display, in a P-channel MOS that switches the column electrodes to the precharge voltage and in a N-channel DMOS that switches the column electrode to low level (ground level or a voltage closed to ground V_{COL_GND}).

The column addressing sequence is divided into 2 different subsequences defined as column discharge/precharge and active period.

5.2.1 Column Pre-charge/Discharge

The column pre-charge occurs at the beginning of each row address period.

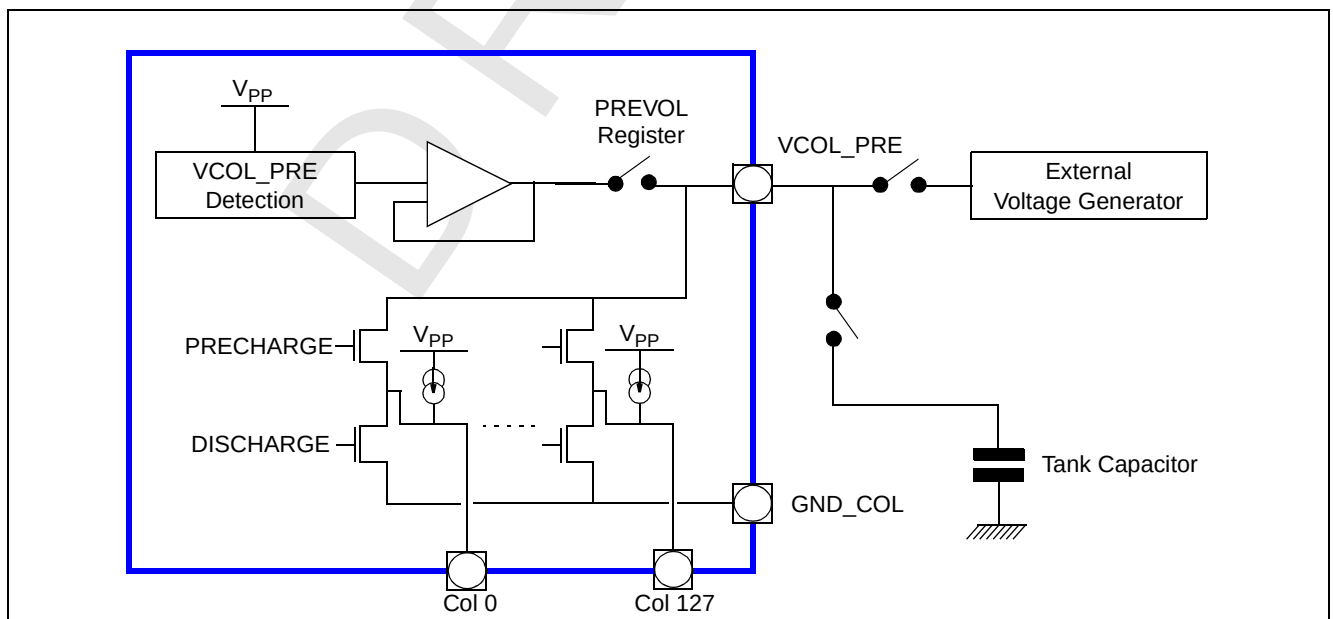
An “off” pixel (black pixel) will be discharged to the ground to block current flowing in the diode (resetting pixel) while the “on” pixel (white pixel) will be precharged closed to the “on” threshold voltage, defined as the precharge voltage (V_{COL_PRE}) before the current flows through the selected “on” row (presetting pixel). The parasitic column capacitance is loaded during the precharge sequence. Using the precharge addressing method improves the efficiency of the display and makes the luminance directly proportional to the column brightness current and current duty-cycle.

Discharging only the “off” pixel reduces capacitance losses.

This is an accurate method that regroups the discharge and precharge sequences, thus increasing the duration of the active cycle.

The optimal precharge voltage presets the diodes at their turn-on point. This voltage is directly related to the brightness level and provides an accurate activation of the pixel diodes. The column current source only provides energy to the pixel diode and does not participate in charging the column capacitance.

Figure 32: Column Driver Voltage Diagram



The precharge voltage V_{COL_PRE} can be selected as:

- an internal voltage adjusted automatically on the brightness level and pixel operating voltages,
- an external voltage connected to the V_{COL_PRE} pins. It is important to note that V_{COL_PRE} must be lower than V_{PP}
- a tank capacitor connected to the V_{COL_PRE} pins. Capacitive currents can be collected to this tank capacitor and used to generate a precharge voltage. This way is less accurate than the internally-generated V_{COL_PRE} .

The precharge voltage options are selected in register PREVOL.

The resulting discharge and precharge waveforms are controlled to prevent too fast transitions.

5.2.2 Active Period

The active period corresponds to the light-emission period. The global brightness setting defines the current delivered by the column driver output stage. The STV8102 allows up to 127 steps of brightness adjustment to set the active current in the column driver.

The column driver output current is a linear function of the reference current defined by:

$$I_{OUT} = I_{REF} \times N, \text{ where } N = 0 \text{ to } 127$$

The maximum brightness in this case is 255 μA .

A high current option selected by the MAX.BRIGHT bit is used to double the current delivered by the column driver.

$$I_{OUT} = (2 \times I_{REF}) \times N, \text{ where } N = 0 \text{ to } 127$$

The maximum brightness in this case is 500 μA .

The output current defined by the brightness adjustment flows through the column electrodes during the active write period. The current sources of the output stage are automatically turned in high impedance mode at the end of the active period during a single internal clock step.

5.3 Optimization of the Column Driving Scheme

To reduce power consumption, the OLED display can be driven with optimized driving schemes adapted to the application requirements.

Register PREDIS_SEL defines the presence (absence) of the discharge and/or precharge or the use of a dedicated sequence without discharge and that connects together all “off” column outputs to collect current losses on the common V_{COL_PRE} node.

Register PREDISDUR defines the duration of precharge and discharge sequences and the temporal position of the signal edges in relation to the row sequence.

The recommended sequence simultaneously performs a precharge for an “on” (white) pixel and a discharge for an “off” (black) pixel. This results in an optimization of the power consumption by reducing the capacitive losses and increasing the active sequence.

However, for each of these modes, the user can force the driving scheme to the following cycles:

1. Pre-charge and discharge
2. No pre-charge, no discharge
3. No Pre-charge, discharge
4. Pre-charge, no discharge

The user can choose between a sequential or parallel mode of the discharge and pre-charge periods.

The row period is divided in 20 cycles which are a Hi-Z period (1 cycle), discharge period (0 or 1 cycle), pre-charge period (1 or 2 cycles), the remaining number of cycles being the active period.

The duration of each pre-charge can be selected between one or two cycles. **It must be noted that the STV8102 operates in a voltage pre-charge mode.**

5.4 Examples of the Row/Column Driving Waveforms

The activation of the precharge/discharge function is done with the PREcharge DIScharge SElection register and the selection of the sequential/parallel scheme and duration is done with the PREDIS DURATION register. (For more information, refer to [Chapter 10: Control and Status Registers Description.](#))

Figure 33: Parallel Precharge/Discharge Scheme (optimized sequence)

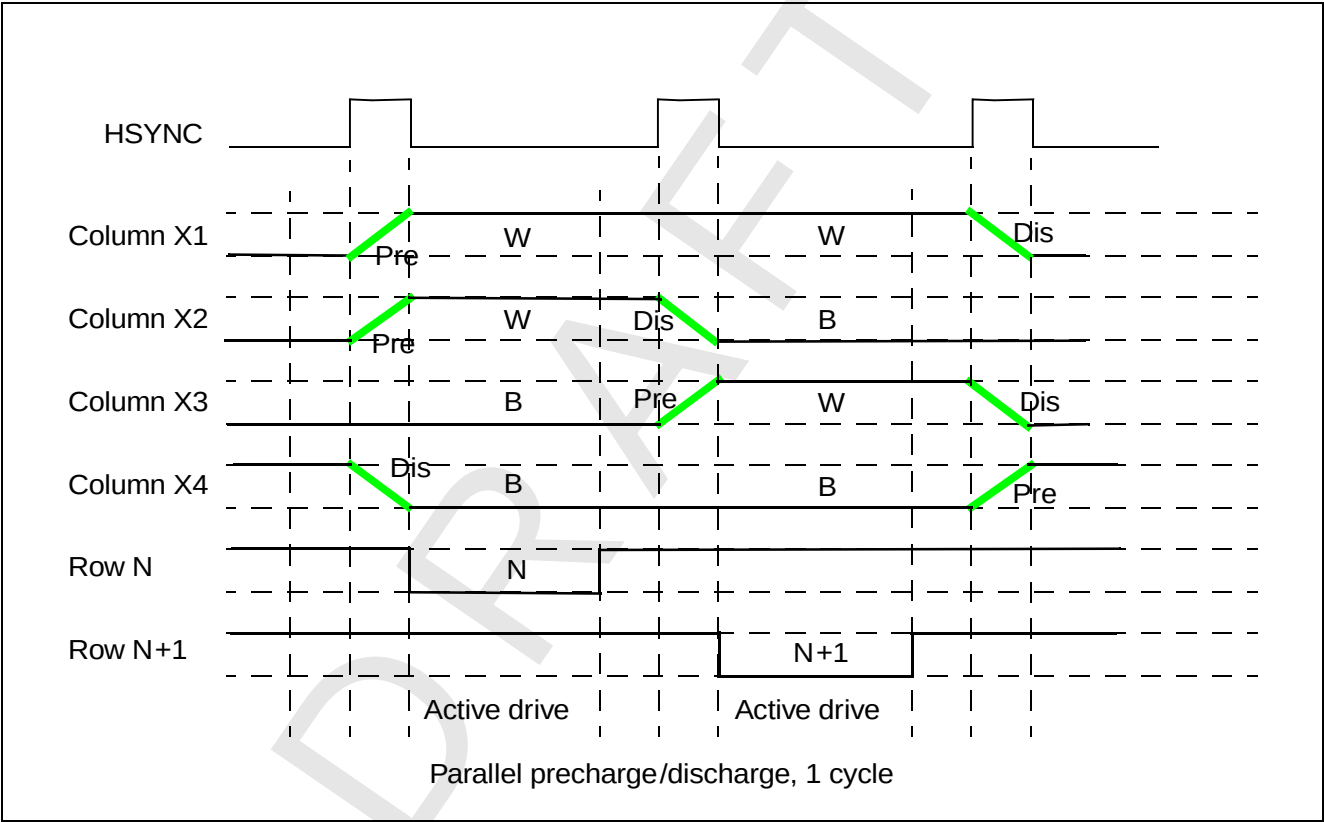


Figure 34: Sequential Precharge/Discharge Scheme

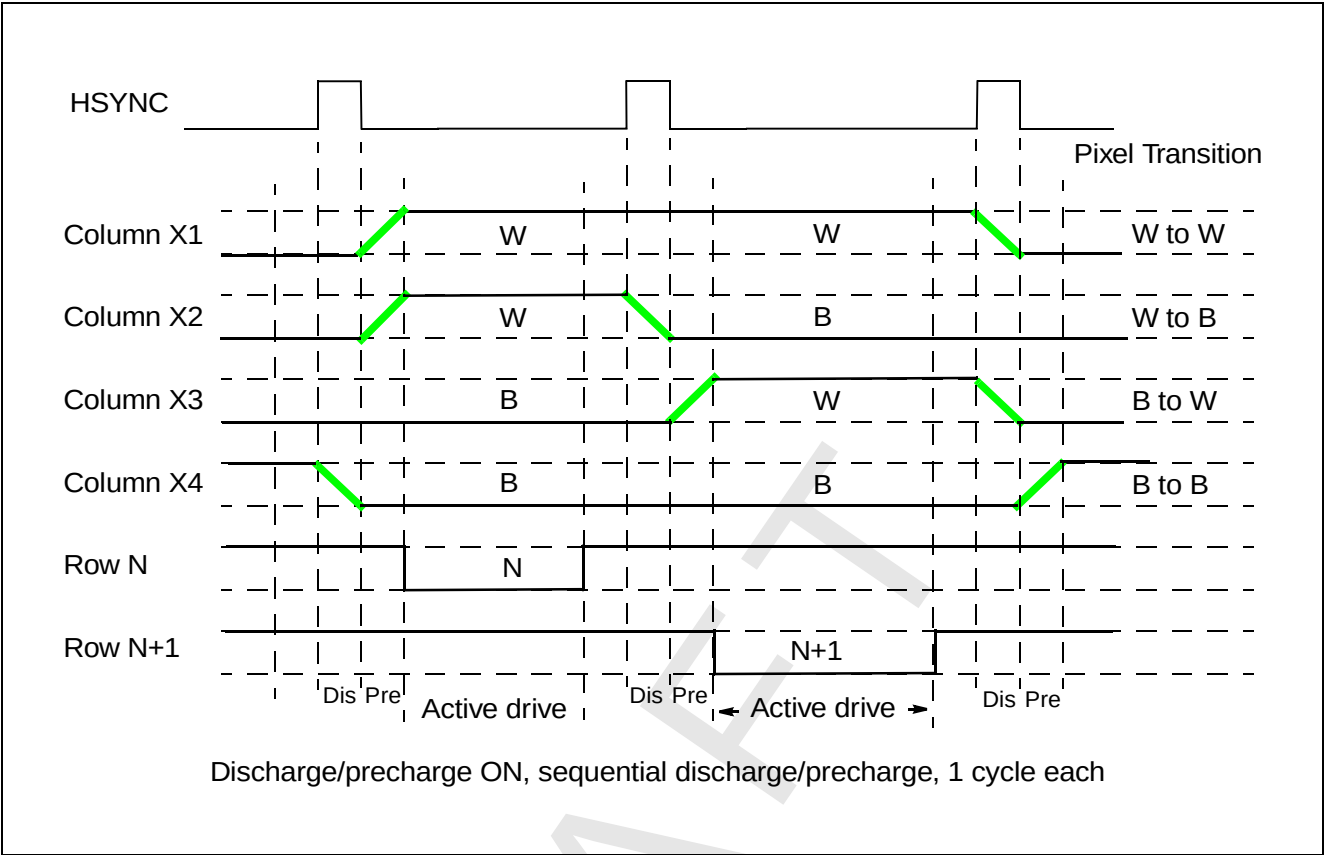
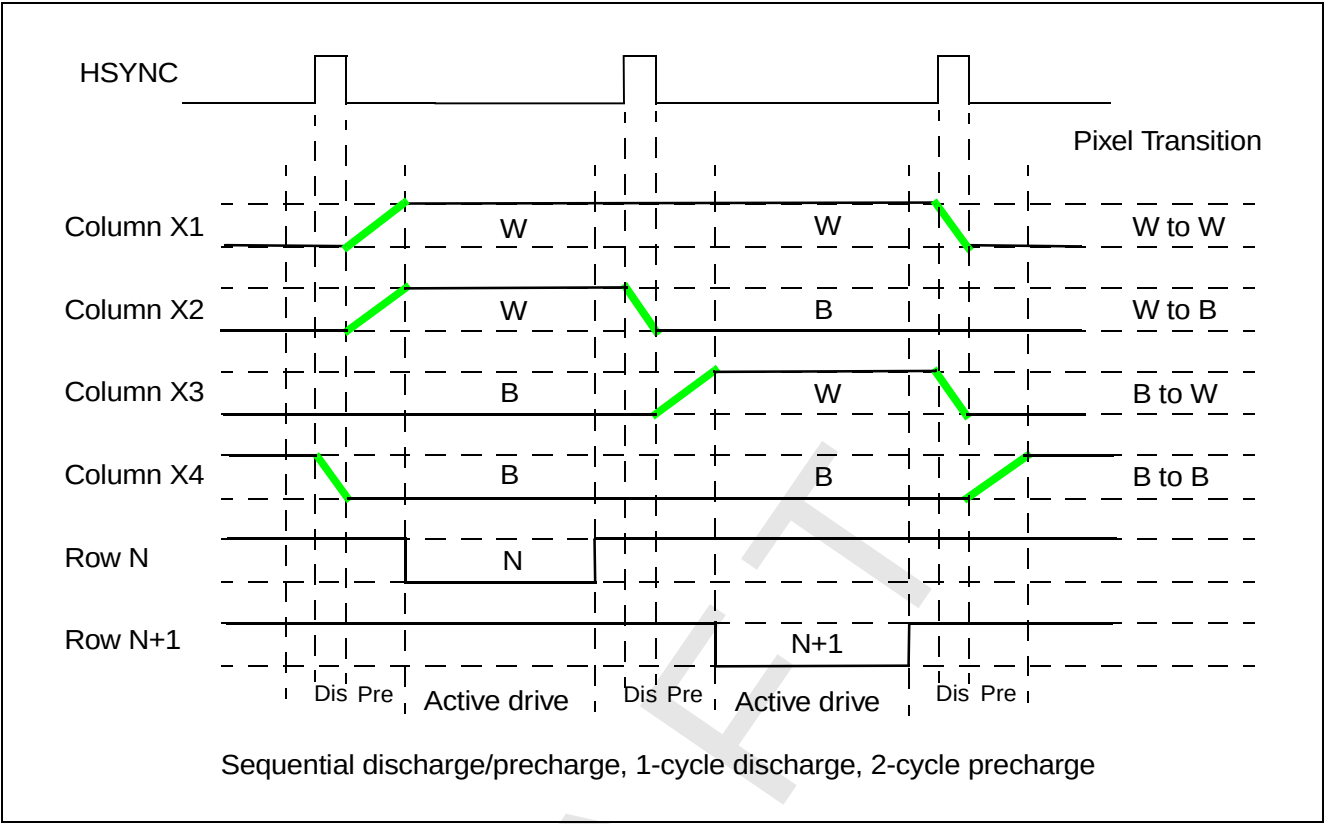


Figure 35: Sequential 2-Cycle Precharge Scheme



6 Scanning Control

The STV8102 features a “Self-adaptive Scanning” processing which leads to adapt the row period to the picture contents. This “Self-adaptive Scanning” drastically decreases the overall display power consumption.

This feature is implemented in the scanning control block which generates the row/column driving signals. The STV8102 can operate in active mode without host processing or in passive mode with host control. The “Self-adaptive Scanning” modes are selected using 2 registers.

The scanning control block monitors the display RAM contents with a resolution of 8 blocks of 8 consecutive rows starting at row 0. A checksum is performed of each frame on each block. If the block holds at least one pixel, the block is displayed, else it is blanked. Only row driver signals corresponding to row drivers blocks with active data are generated. The line duration is adapted to the number of active rows, while the frame frequency remains unchanged to minimize system power consumption.

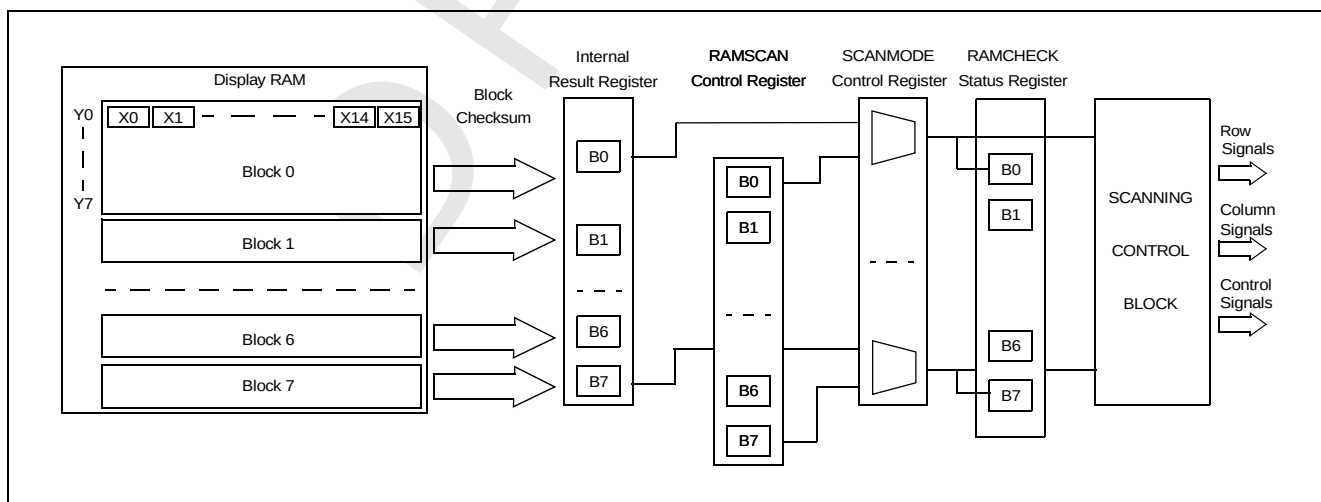
The **active mode** is selected by “clearing” the $\overline{\text{AUTO}}$ bit of the SCANMODE register. The STV8102 then automatically runs the “Self-adaptive Scanning”, driving the panel at the lowest line frequency to minimize power consumption. In addition, the driving current is also decreased in the same ratio which results in a further decrease of power consumption and to an increase in the lifetime of the panel. Reading the RAMCHECK register gives the block status.

The **passive mode** is selected by “setting” the $\overline{\text{AUTO}}$ bit of the SCANMODE register. The host can then check the contents of 8 blocks in the display RAM by reading the RAMCHECK register and decide to blank, or not, some of the 8 row blocks by writing to the RAMSCAN control register. The line frequency is adapted accordingly (see Figure 36).

In either active or passive mode, the adjustment of the line frequency requires a fine-tuning of the column current to keep a constant luminance level on the panel. This fine-tuning is automatically controlled by the logic control block through the ‘Current Management’ block.

The ‘Current Management’ block generates the reference current for the column driver stage.

Figure 36: Self-adaptive Scanning Block Diagram



7 Power Supply Management - Powermizer™

The STV8102 has an enhanced power supply control scheme named **Powermizer™**.

The 'Power Supply Management' block controls the external step-up circuitry that generates the high-voltage supply (V_{PP}) for the panel (see [Figure 37](#)). The STV8102 continuously controls the step-up circuitry to regulate the V_{PP} supply and the derived V_{COL_PRE} precharge and V_{ROW_OFF} row-off internal voltages. The control loop tracks the panel operating characteristics and adjusts the power supply to ensure minimum power dissipation independently of the OLED/LEP material characteristics over time and temperature. This function is particularly interesting in case of strong brightness decrease. In this type of configuration, the driving voltage of the display is always adapted to the optimum pixel operating voltage. If the STV8102 is powered with an external fixed V_{PP} supply, the power supply management must be disabled.

The column pre-charge voltage is internally generated. V_{COL_PRE} is set [1.5V to 2V] below V_{PP} . If V_{COL_PRE} is externally supplied, the internal generation must be disabled using the PREVOL register. It is also possible to connect an external capacitor to the V_{COL_PRE} pin. The column pre-charge voltage is then an average of the ON voltage of the display.

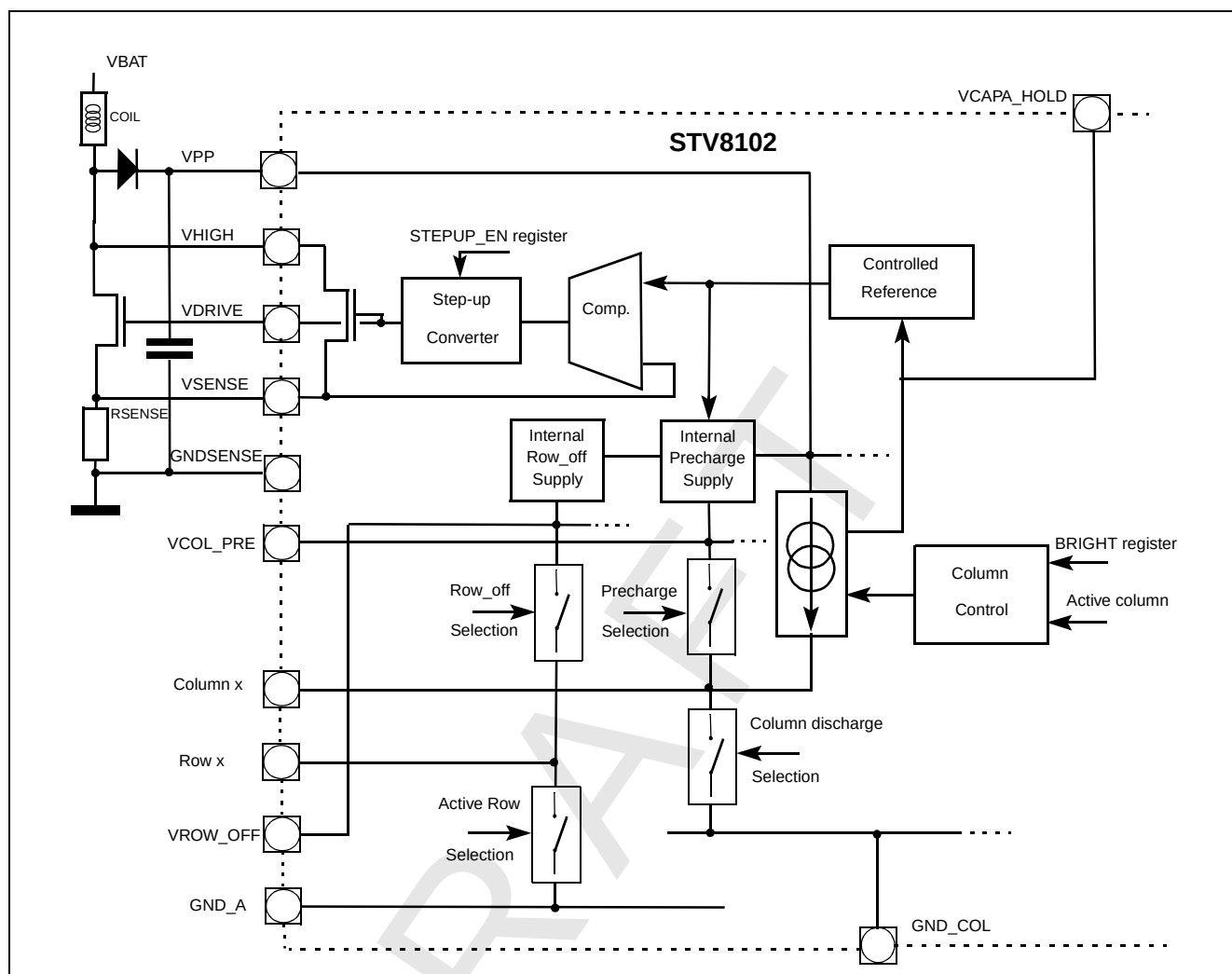
The same configuration is valid for the V_{ROW_OFF} row-off voltage. (See register ROWOFFVOL.)

These different operating modes are defined by registers (see [Chapter 10: Control and Status Registers Description](#)).

The DC-to-DC Converter is a step-up converter with an input voltage V_{BATT} and an output voltage V_{PP} (from 5 to 18V). The switching frequency (350kHz, typ.) is internally generated.

During start-up, V_{PP} equals $V_{BATT} - V_{DIODE}$ and an internal NMOS transistor connected between pins VHIG and VDRIVE allows V_{PP} to rise until the voltage on pin VDRIVE (stemming from V_{PP}) is high enough to switch the external NMOS transistor. Both the internal and external NMOS transistors work in parallel. The external NMOS transistor is always required. The internal NMOS transistor is not sized to switch the normal operating current of the application.

Figure 37: Power Supply Management Block Diagram



8 Oscillator – Timing Generator

The 'Oscillator, Timing Generator' block generates the internal clocks for the STV8102 digital blocks. The reference clock can be fed externally on the EXT-CLK pin or come internally from the on-chip oscillator. The necessary signals are generated to control the external DC-to-DC converter and all the scanning signals.

Figure 38 shows the timing generator block diagram.

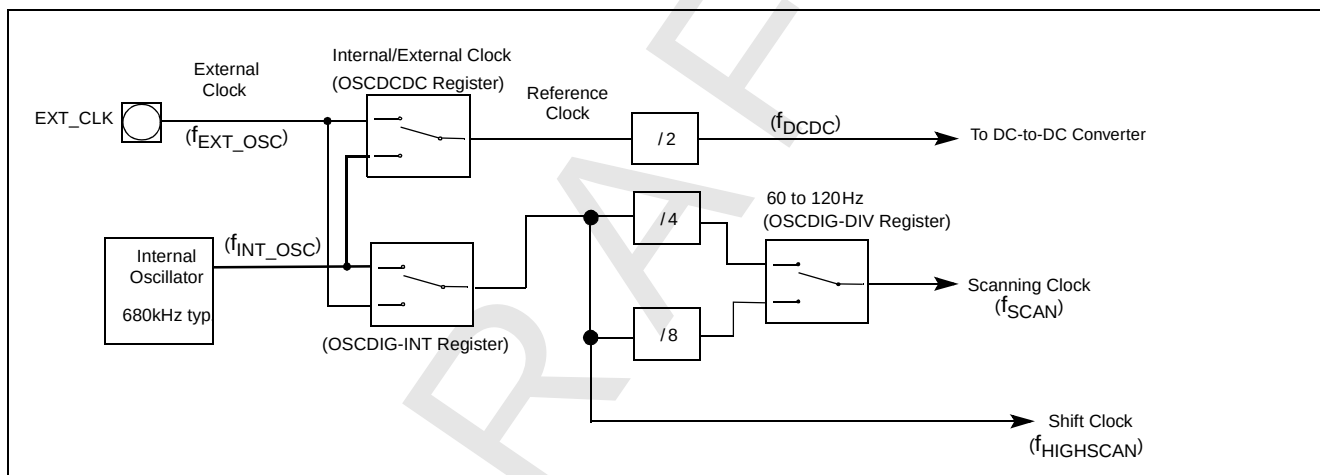
Different commands can be used to adapt the timing generator to several configurations (See Register Description chapter).

The DC-to-DC converter clock (f_{DCDC}) is half the frequency of the selected reference clock.

The frame and row clocks can be automatically or manually adapted to the display mode (full picture, screen saver, ...).

A basic scanning clock period (f_{SCAN}) of 1/20th the row period is used to run the selected column sequence (precharge, discharge, ...) The row period is automatically controlled by the scanning block to fit the running display mode (active, screen saver, ...) and the selected frame rate.

Figure 38: Timing Generator Block Diagram



The frame duration is:

$$f_{\text{FRAME}} = f_{\text{ROW}} / 64^*$$

$$f_{\text{ROW}} = f_{\text{SCAN}} / 20^*$$

Using a typical internal reference clock frequency of 680kHz ($f_{\text{INT_OSC}}$):

- a 60Hz (minimum) frame frequency is obtained by a division rate of 8
 $f_{\text{SCAN}} = 85\text{kHz}^*$, $f_{\text{ROW}} = 4.25\text{kHz}^*$ and $f_{\text{FRAME}} = 66\text{Hz}^*$
 - a 120Hz (minimum) frame frequency is obtained by a division rate of 4
 $f_{\text{SCAN}} = 170\text{kHz}^*$, $f_{\text{ROW}} = 8.5\text{kHz}^*$ and $f_{\text{FRAME}} = 132\text{Hz}^*$
- * With 64 rows active

If the Self-adaptive Scanning system skips some blank rows, the row frequency decreases but the frame frequency remains close to the selected value.

In case the factor 4 is used (to run at a higher frame frequency), the screen saver mode can operate in or on a reduced area.

9 STV8102 Configuration

The STV8102 provides a set of registers to configure the device to the hardware of the display. This chapter gives a summary of the controller state after a hardware reset and provides an example of configuration to adapt the controller to a given screen.

9.1 Reset Configuration

Before starting operation, a configuration sequence must initialize the STV8102 registers with a set of values in accordance with the application and with the display hardware. The register initialization sequence is loaded through the bus interface. When enabled, the selected interface (with SEL0, SEL1) can operate using the interface signals provided by the host.

The configuration has to be performed during the software initialization sequence by the host after any reset.

The default configuration of the STV8102 after a hardware reset is:

- all the control registers are cleared (display OFF, DC-DC step-up OFF, internal oscillator OFF, scanning OFF),
- the RAM contents are unchanged (on Power ON: RAM contents are defined)

Note: the hardware reset must be applied all the power-up sequence long, until the supplies reach the minimum value specified in [Chapter 11: Electrical Characteristics](#).

9.2 Display OFF Configuration

After the Display OFF command the configuration is as follows:

- Internal registers unchanged
- RAM unchanged
- Internal oscillator is inactive
- DC-DC step-up is OFF

9.3 Example Configuration

This section describes an example of a standard “like” configuration. This configuration is sent in order to have a normally functioning display. It is listed below in [Table 19: Configuration Sequence](#) and corresponds to the display of [Figure 39](#).

The configuration sequence brings the necessary flexibility to adapt the generated signals to the hardware and the characteristics of the screen.

The values of registers used in the example are given in two ways, the binary/hexadecimal value when applicable or the bit name/position/value and the name of the corresponding register when needed. Only registers implied in the configuration are documented (with type name = “config” in the Control and Status Register chapter). The resulting pin assignment is summarized in the corresponding [Figure 39](#). Registers not mentioned keep their default reset value.

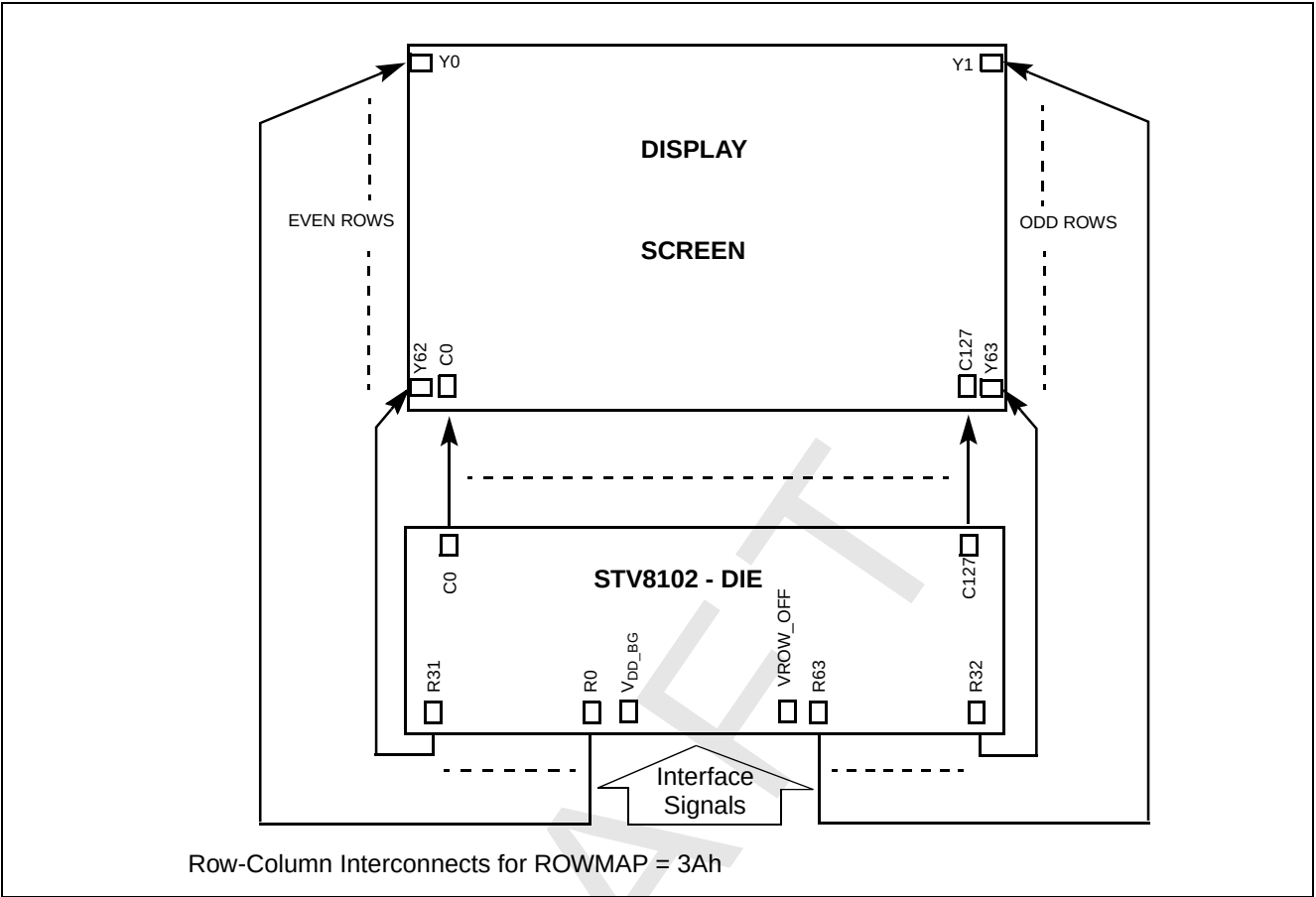
Refer to the Control and Status Register chapter for the detailed register description.

Screen features: The columns start from 0 to 128, left to right, at the bottom of the screen. The even rows start from 0 to 62, top to bottom, on the left side and odd rows from 1 to 63, top to bottom, on the right side.

Table 19: Configuration Sequence

Register Name	Value	Description
OSCCTRL	12h	Internal clock/internal oscillator enabled/divide by 8 (60Hz)
STEPUP_EN	19h	Step-up converter enabled
PREDIS_SEL	26h	With precharge/with discharge
ROWHIZ	28h	Inactive rows to VROW_OFF
EXTMOS_EN	2Bh	External MOS enabled
PREVOL	2Ch	Internal precharge supply
ROWOFFVOL	2Eh	Internal row_off supply
ROWMAP	3Ah	Row mapping, see Figure 39
VPPCLAMP	A614h	Set Vpp clamp value
PIXLMAP	B1h	Fill RAM using bit7 as MSB
BRIGHT	CE19h	Setup Brightness value
PREDISDUR	D020h	Parallel precharge/discharge mode
DISPON	AFh	Turn display on

Figure 39: Row - Column Assignment



10 Control and Status Registers Description

The STV8102 has a set of control and status registers to configure and monitor the display system. They are accessed with the interface bus as described in [Chapter 2: Bus Interfaces](#).

The display RAM, organized as a byte array, is also accessed in write mode through the interface bus with the selection of the SD/C pin at "1". It is described in [Chapter 3: Display RAM](#).

The following rules are used in this datasheet to describe bits, bit-fields and registers:

- SPICCTRL is the register name,
- FADON.SPICCTRL is the FADON bit of the SPICCTRL register,
- EFFECT.SPICCTRL is the EFFECT bit-field of the SPICCTRL register.

Unused bits are read as 0 and must be written at 0.

In the following sections the registers are described with the same rules. The reset default values are given and the bit or bit-fields are detailed.

10.1 Register Map

Table 20: List of Registers (Sheet 1 of 2)

Name	msb														lsb
XSTART	0	0	0	0	XSTART[3:0]										
OSCCTRL	0	0	0	1	0	EXT/ INT	OSC ON	DIV							
STEPUP_EN	0	0	0	1	1	0	0	STEPUP_EN							
PREDIS_SEL	0	0	1	0	0	PREDIS_SEL[2:0]									
ROWHIZ	0	0	1	0	1	0	0	ROWHIZ							
EXTMOS_EN	0	0	1	0	1	0	1	EXTMOS_EN							
PREVOL	0	0	1	0	1	1	0	PREVOL							
ROWOFFVOL	0	0	1	0	1	1	1	ROWOFFVOL							
ROWMAP	0	0	1	1	ROWMAP[3:0]										
YSTART	0	1	YSTART[5:0]												
MOVE	1	0	0	0	HMOVE[1:0]		VMOVE[1:0]								
HSPEED	1	0	0	1	0	HSPEED[2:0]									
VSPEED	1	0	0	1	1	VSPEED[2:0]									
HVEN	1	0	1	0	0	0	0	HVEN							
INVIDEO	1	0	1	0	0	0	1	INVID							
VPPCLAMP	1	0	1	0	0	1	1	0	0	0	0	VPPCLAMP[4:0]			
DISPON	1	0	1	0	1	1	1	DISPON							
PIXLMAP	1	0	1	1	0	B2T	R2L	MSB							
RAMROW	1	0	1	1	1	0	0	RAMROW							
SCANMODE	1	0	1	1	1	0	1	AUTO							
HMIN	1	1	0	0	0	0	0	0	HMIN[7:0]						
HMAX	1	1	0	0	0	0	1	0	HMAX[7:0]						

Table 20: List of Registers (Sheet 2 of 2)

Name	msb																lsb
HSHIFT	1	1	0	0	0	1	0	0	HSHIFT[7:0]								
VMIN	1	1	0	0	0	1	1	0	0	VMIN[6:0]							
VMAX	1	1	0	0	1	0	0	0	0	VMAX[6:0]							
VSHIFT	1	1	0	0	1	0	1	0	0	VSHIFT[6:0]							
RAMSCAN	1	1	0	0	1	1	0	0	RAMSCAN[7:0]								
BRIGHT	1	1	0	0	1	1	1	0	MAX	BRIGHT[6:0]							
PREDISUR	1	1	0	1	0	0	0	0	0	SEP	DISEL	CYC	0	0	0	0	
PATTERN_EN	1	1	0	1	0	1	1	PATEN									
PATTERN_SEL	1	1	0	1	1	SEL[2:0]											
NOP	1	1	1	0	0	0	1	0									
RAMCHECK	1	1	1	0	1	1	0	0	RAMSCANCHECK[7:0]								
IDCHIP	1	1	1	0	1	1	1	0	IDCHIP[7:0]								

10.2 Register Description Ordered by Name

BRIGHT - W - Brightness Range Selection

Default value: 00h

Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

Command code								Data							
CEh								MAX	BRIGHT[6:0]						

Bit Name	Reset	Function
MAX	0	Brightness Range Selection (I_{BRX}) 0: I _{BR1} selection - 250uA 1: I _{BR2} selection - 500uA
BRIGHT[6:0]	000 0000b	Brightness Value 000 0000b: 0 000 0001b: 1/127 of I _{BRx} xxx xxxxb: -1 row shift to the bottom 111 1111b: I _{BRx} max value

DISPON - W - Display Enable

Default value: AEh

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

1	0	1	0	1	1	1	DISPON
---	---	---	---	---	---	---	--------

Bit Name	Reset	Function
DISPON	0	Display Enable 0: Disable, Blank Screen 1: Enable

EXTMOS_EN - W - External MOS Enable**Default value: 2Ah**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	1	0	1	EXTMOS_EN

Bit Name	Reset	Function
EXTMOS_EN	0	External Power MOSFET Enable 0: Disabled 1: External MOS Enabled

HMAX - W - Horizontal Left Shift Limit**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code									Data						
C2h									HMAX[7:0]						

Bit Name	Reset	Function
HMAX[7:0]	00h	Horizontal Left Shift Limit 80h: -128 pixel shift to the left ----- FFh: -1 pixel shift to the left 00h: no shift 01h: 1 pixel shift to the right ----- 7Fh: 127 pixel shift to the right

HMIN - W - Horizontal Right Shift Limit**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code									Data						
C0h									HMIN[7:0]						

Bit Name	Reset	Function
HMIN[7:0]	00h	Horizontal Right Shift Limit 80h: -128 pixel shift to the left ----- FFh: -1 pixel shift to the left 00h: no shift 01h: 1 pixel shift to the right ----- 7Fh: 127 pixel shift to the right

HSHIFT - W - Horizontal Shift Selection**Default value: 00h**

Bit 15 Bit 14 Bit 13 Bit 12 Bit 11 Bit 10 Bit 9 Bit 8 Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

Command code	Data
C4h	HSHIFT[7:0]

Bit Name	Reset	Function
HSHIFT[7:0]	00h	Horizontal Shift Selection 80h: -128 pixel shift to the left ----- FFh: -1 pixel shift to the left 00h: No shift 01h: 1 pixel shift to the right ----- 7Fh: 127 pixel shift to the right

HSPEED - W - Screen Saver Horizontal Speed**Default value: 90h**

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

1	0	0	1	0	HSPEED[2:0]		
---	---	---	---	---	-------------	--	--

Bit Name	Reset	Function
HSPEED[2:0]	000b	Horizontal Moving Speed selection 000: no shift, no motion 001: shift to HSHIFT and move 1 step to the right every 3 frame 010: shift to HSHIFT and move 1 step to the right every 2 frames 011: shift to HSHIFT and move 1 step to the right every 1 frames 100: shift to HSHIFT, no motion 101: shift to HSHIFT and move 1 step to the left every 3 frames 110: shift to HSHIFT and move 1 step to the left every 2 frames 111: shift to HSHIFT and move 1 step to the left every 1 frame

HVEN - W - Horizontal/Vertical Enable**Default value: A0h**

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

1	0	1	0	0	0	0	HVEN
---	---	---	---	---	---	---	------

Bit Name	Reset	Function
HVEN	0	Horizontal/Vertical Enable 0: Disabled 1: Horizontal/Vertical Enable

IDCHIP - R - Chip Identification**Value: 07h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
EEh								IDCHIP[7:0]							

Bit Name	Fixed Value	Function
IDCHIP[7:0]	07h	IDchip = 0111b

INVIDEO - W - Inverse Video Enable**Default value: A2h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	0	0	0	1	INVIDEO

Bit Name	Reset	Function
INVIDEO	0	Inverse Video Enable 0: Disabled 1: Inverse Video Enabled

MOVE - W - Screen Saver Effect Selection**Default value: 80h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	0	HMOVE[1:0]	VMOVE[1:0]		

Bit Name	Reset	Function
HMOVE[1:0]	00b	Horizontal Moving Effect selection 00: Limit to Limit 01: Bounce Only 10: Wrap Only 11: Bounce and Wrap
VMOVE[1:0]	00b	Vertical Moving Effect selection 00: Limit to Limit 01: Bounce Only 10: Wrap Only 11: Bounce and Wrap

OSCCTRL - W - Clock Control Register

Default value: 14h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	0	EXT/ $\overline{\text{INT}}$	OSC ON	DIV

Bit Name	Reset	Function
EXT/ $\overline{\text{INT}}$	0	Clock Selection 0: Internal 1: External
OSC ON	1	Internal Oscillator Enable 0: Disabled 1: Enabled
DIV	0	Reference Clock Divider selection 0: Divided by 8 -> 60Hz 1: Divided by 4 -> 120Hz but display panning and screen saver functions are disabled, see remark in Section 4.3 and in Section 4.4

PATTERN_EN - W - Pattern Enable

Default value: D6h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	1	0	1	1	PATEN

Bit Name	Reset	Function
PATEN	0	Pattern Enable 0: Disabled 1: Pattern Enabled

PATTERN_SEL - W - Pattern Select

Default value: D8h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	1	1	SEL		

Bit Name	Reset	Function
SEL	000b	Pattern Select 000b: blank screen, refer to Table 18: Display Pattern Selection 001b: black and white columns, refer to Table 18: Display Pattern Selection 010b: checker board pattern, refer to Table 18: Display Pattern Selection ----- 111b: white screen, refer to Table 18: Display Pattern Selection

PIXLMAP - W - Mirror Effect Selection**Default value: B1h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	1	0	B2T	R2L	MSB

Bit Name	Reset	Function
B2T	0	Vertical Display selection 0: top to bottom display (normal vertical display, display corresponds to RAM contents) 1: bottom to top display (display reversed compared to RAM contents)
R2L	0	Horizontal Display selection 0: left to right display (normal horizontal display, display corresponds to RAM contents) 1: right to left display (display reversed compared to RAM contents)
MSB	1	MSB Receive Position (RAM write only) Serial interfaces 0: MSB is the 8th received bit 1: MSB is the 1st received bit Parallel interfaces MSB is Bit[0] MSB is Bit[7] RAM data write only default value

PREDISUR - W - Parallel or Sequential Pre/Discharge Selection**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
D0h								0	SEP	DISEL	CYC	0	0	0	0

Bit Name	Reset	Function
SEP	0	Parallel or Sequential Precharge/Discharge selection 0: Parallel Precharge/Discharge (in the same cycle) 1: Sequential Precharge/Discharge (different cycles)
DISEL	0	Discharge mode 0: All columns discharged (in the same cycle) 1: Selective discharge (only white to black transition columns)
CYC	0	Precharge cycle selection 0: 1 cycle long precharge 1: 2 cycles long precharge
Bits[3:0]	0000b	Reserved , must be kept to 0000b

PREDIS_SEL - W - Precharge/Discharge Selection**Default value: 20h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	0	PREDIS_SEL[2:0]		

Bit Name	Reset	Function
PREDIS_SEL[2:0]	000b	All Column Precharge Discharge selection * 000: No Precharge, No Discharge 001: No Precharge, No Discharge, Off pixels connected to V _{COL_PRE} 010: With Precharge, No Discharge 011: Not used. 100: no precharge, with discharge 101: Not used. 110: with precharge, with discharge 111: Not used.

* Enable with PREDISDUR.DISEL = 1 only.

PREVOL - W - Precharge Supply Selection

Default value: 2Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	1	1	0	PREVOL

Bit Name	Reset	Function
PREVOL	0	Precharge Supply selection 1: External supply on pin V _{COL_PRE} 0: Internal precharge supply

RAMCHECK - R - Row Block Checksum Result

Reset value: 00h

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
ECh								RAMSCANCHECK[7:0]							

Bit Name	Reset	Function
RAMSCANCHECK[7:0]	00h	8 Row Block Checksum Result Bit 7: Block 7, lines 56 to 63 Bit 6: Block 6, lines 48 to 55 Bit 5: Block 5, lines 40 to 47 Bit 4: Block 4, lines 32 to 39 Bit 3: Block 3, lines 24 to 31 Bit 2: Block 2, lines 16 to 23 Bit 1: Block 1, lines 8 to 15 Bit 0: Block 0, lines 0 to 7 When a bit is set, the corresponding block is activated. When the bit is reset, the corresponding block is blanked. Example: FFh means that all blocks are activated.

RAMROW - W - RAM Access in Row Mode**Default value: B8h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	1	1	0	0	RAMROW

Bit Name	Reset	Function
RAMROW	0	Access the RAM in Row Access mode 0: Disable 1: Enable

RAMSCAN - W - ROW Block Blanking**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
CCh								RAMSCAN[7:0]							

Bit Name	Reset	Function
RAMSCAN[7:0]	00h	8 Row Block Blanking Bit 7: Block 7, lines 56 to 63 Bit 6: Block 6, lines 48 to 55 Bit 5: Block 5, lines 40 to 47 Bit 4: Block 4, lines 32 to 39 Bit 3: Block 3, lines 24 to 31 Bit 2: Block 2, lines 16 to 23 Bit 1: Block 1, lines 8 to 15 Bit 0: Block 0, lines 0 to 7 When a bit is set, the corresponding block is activated. When the bit is reset, the corresponding block is blanked. Example: FFh means that all blocks are activated.

ROWHIZ - W - Row OFF Selection Register**Default value: 28h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	1	0	0	ROWHIZ

Bit Name	Reset	Function
ROWHIZ	0	ROW HiZ selection 0: Off-rows switched to V_{ROW_OFF} 1: Inactive or off-rows in High Impedance state.

ROWMAP - W - Row Mapping Selection**Default value: 30h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	1	ROWMAP[3:0]			

Bit Name	Reset	Function
ROWMAP[3:0]	0000b	Row Mapping on Driver Output Pin R0 to R31 pin R32 to R63 driver outputs 0000: line 0 to 31 line 32 to 63 continuous set 0001: line 1, 3,...to 63 line 0, 2,...to 62 odd set and even set 0010: line 0, 2,...to 62 line 1, 3,...to 63 even set and odd set 0011: line 32 to 63 line 0 to 31 continuous set 0100: line 31 to 0 line 63 to 32 continuous set 0101: line 63, 61,...to 1 line 62, 60,...to 0 odd set and even set 0110: line 62, 60,...to 0 line 63, 61,...to 1 even set and odd set 0111: line 63, 62,...to 32 line 31, 30,...to 0 continuous set 1000: line 0 to 31 line 63 to 32 continuous set 1001: line 1, 3,...to 63 line 62, 60,...to 0 odd set and even set 1010: line 0, 2,...to 62 line 63, 61,...to 1 even set and odd set 1011: line 32 to 63 line 31 to 0 continuous set 1100: line 31 to 0 line 32 to 63 continuous set 1101: line 63, 61,...to 1 line 0, 2,...to 62 odd set and even set 1110: line 62, 60,...to 0 line 1, 3,...to 63 even set and odd set 1111: line 63, 62,...to 32 line 0, 1,...to 31 continuous set

ROWOFFVOL - W - Row OFF Supply Selection**Default value: 2Eh**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	1	0	1	1	1	ROWOFFVOL

Bit Name	Reset	Function
ROWOFFVOL	0	Discharge Supply selection 1: External supply on pin VROW_OFF 0: Internal row-off supply

SCANMODE - W - Self-adaptive Scanning Selection**Default value: BAh**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	1	1	1	0	1	AUTO

Bit Name	Reset	Function
AUTO	0	Self-adaptive Scanning enable 1: Disable, passive mode, the host reads RAMCHECK and selects the rows with RAMSCAN 0: Enable, automatic blanking of the black row blocks

STEPUP_EN - W - Setup Converter Control Register**Default value: 18h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	1	0	0	STEPUP_EN

Bit Name	Reset	Function
STEPUP_EN	0	Step-up Converter selection 0: external supply on V _{PP} 1: step-up converter enabled, internally generated supply

VMAX - W - Vertical Bottom Shift Limit**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
C8h								0	VMAX[6:0]						

Bit Name	Reset	Function
VMAX[6:0]	00h	Vertical Bottom Shift Limit (bit 7 must be kept to 0) 40h: -64 row shift to the bottom ----- 7Fh: -1 row shift to the bottom 00h: no shift 01h: 1 row shift to the top ----- 3Fh: 63 row shift to the top

VMIN - W - Vertical Top Shift Limit**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
C6h								0	VMIN[6:0]						

Bit Name	Reset	Function
VMIN[6:0]	00h	Vertical Top Shift Limit (bit 7 must be kept to 0) 40h: -64 row shift to the bottom ----- 7Fh: -1 row shift to the bottom 00h: no shift 01h: 1 row shift to the top ----- 3Fh: 63 row shift to the top

VPPCLAMP - W - VPP Clamp Value**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
A6h								0	0	0	VPPCLAMP[4:0]				

Bit Name	Reset	Function
VPPCLAMP[4:0]	0 0000b	VPP Clamp Value * 0 0000b: 5V, the min. VPP clamp value - corresponds to max. OLED display protection 0 0001b: 5.42V ----- 1 00 00b: 11.7V ----- 1 1110b: 17.58V 1 1111b: 18V, the max. VPP clamp value - corresponds to min. OLED display protection

* under the recommended operating conditions of [Section 11.3](#)

VSHIFT - W - Vertical Shift Selection**Default value: 00h**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command code								Data							
CAh								0	VSHIFT[6:0]						

Bit Name	Reset	Function
VSHIFT[6:0]	00h	Vertical Shift Selection (bit 7 must be kept to 0) 40h: -64 row shift to the bottom ----- 7Fh: -1 row shift to the bottom 00h: no shift 01h: 1 row shift to the top ----- 3Fh: 63 row shift to the top

VSPEED - W - Screen Saver Vertical Speed**Default value: 98h**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	1	VSPEED[2:0]		

Bit Name	Reset	Function
VSPEED[2:0]	000b	Vertical Moving Speed selection 000: no shift, no motion 001: shift to VSHIFT and move 1 step to the bottom every 3 frame 010: shift to VSHIFT and move 1 step to the bottom every 2 frames 011: shift to VSHIFT and move 1 step to the bottom every 1 frames 100: shift to VSHIFT, no motion 101: shift to VSHIFT and move 1 step to the top every 3 frames 110: shift to VSHIFT and move 1 step to the top every 2 frames 111: shift to VSHIFT and move 1 step to the top every 1 frame

XSTART - W - RAM Write Column Register

Default value: 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	XSTART[3:0]			

Bit Name	Reset	Function
XSTART[3:0]	0000b	RAM Write Column Start Position 0000b: Byte X0, column 0 to 7 0001b: Byte X1, column 8 to 15 ----- 1111b: Byte X15, column 120 to 127

YSTART - W - RAM Write Row Start Position

Default value: 40h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	YSTART[5:0]					

Bit Name	Reset	Function
YSTART[5:0]	000000b	RAM Write Row Start Position 00 0000b: Row 0 00 0001b: Row1 ----- 11 1111b: Row 15?

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Maximum ratings are the values beyond which damage to the device may occur. Functional operation should be restricted to the limits defined in the electrical characteristics table.

Symbol	Parameter	Value	Unit
V_{DD_D} / V_{DD_A}	Low Voltage Supply Range	-0.3, +4.6	V
V_{BATT}	High Voltage Supply Range	-0.3, +6	V
V_{PP}	Analog Display Supply Range	-0.3, +22	V
I_{PP}	DC Display Current Range	64	mA
V_{INPUT}	Logic Input Voltage Range	-0.3, $V_{DD}+0.3$	V
I_{INPUT}	DC Logic Input Current Range	10	mA
P_d	Total Power Dissipation	TBD	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-50, +150	°C

11.2 Thermal Data

Symbol	Parameter	Value	Unit
R_{thJA}	Junction-ambient Thermal Resistance (Maximum) on a single-layer board	TBD	°C/W

11.3 Recommended Operating Conditions

$V_{DD_D} = 3.3V$, $V_{DD_A} = 3.3V$, $V_{PP} = 15V$, $V_{BATT} = 4.2V$, $GND_A = GND_D = GND_S = 0V$, $T_{AMB} = 25^{\circ}C$, $f_{FRAME} = 60Hz$, unless specified otherwise

11.3.1 DC Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{BATT}	High Voltage Supply		2.7		5.0	V
V_{DD_A}, V_{DD_D}	Controller Supply		1.8		3.6	V
V_{PP}	Display Supply	$V_{BATT} < V_{PP}$	5.0	12	20	V
I_{STAND_BY}	Stand-by Current	Device biased but not operating (reset or display off mode)			5	μA
I_{DD_D}	Digital Supply Current					mA
I_{DD_A}	Analog Supply Current					mA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{PP}	Display Supply Current				64	mA
V_{IL}	Low level of input logic signal		GND_D		$0.3 \times V_{DD_D}$	V
V_{IH}	High level of input logic signal		$0.7 \times V_{DD_D}$		V_{DD}	V
I_{IL}	Low level Input current of logic signals	$V_{IL}=0$			1	μA
I_{IH}	High level Input current of logic signals	$V_{IH}=0$			1	μA
V_{COL_GND}	Column low-voltage reference	$V_{DD_A}=3.3V$ $V_{DD_A}=1.8V$	0 0		1.5 0.4	V

11.3.2 Timing Generator

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{INT_OSC}	Frequency of Internal clock oscillator			680	-	kHz
f_{EXT_OSC}	Frequency of external clock signal.		600		1400	kHz
f_{HSYNC}	Row Frequency		0.48		7.68	kHz
f_{VSYNC}	Frame Frequency		60		120	Hz

11.3.3 Row Drivers

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{ROW}	Sink row Supply Current	Maximum Brightness			64	mA
V_{ROW_ON}	ROW_ON Voltage drop	$I_{ROW}=64mA$, $V_{DD_A}=3.3V$		0.5		V
R_{ROW_OFF}	$R_{DS(on)}$ of Row high-side transistor	$V_{DD_A}=3.3V$		350		ohm

11.3.4 Column Drivers

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{COL}	Column Supply Current	Minimum Brightness Maximum Brightness		-5 -500		μA
R_{COL_PRE}	Column output impedance during precharge			750		ohms
R_{COL_DIS}	Column output impedance during discharge	$V_{DD_A}=3.3V$, $V_{GND_COL}=0V$		280		ohms
D_{COL}	Column differential uniformity $D_{COL} = \text{ABS}(I_{COL_N} - I_{COL_N+1})/I_{AVG1}$, $I_{AVG1} = (I_{COL_N} + I_{COL_N+1})/2$	$-250\mu A < I_{COL} < -500\mu A$ $-50\mu A < I_{COL} < -250\mu A$		1 5		%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
D_{CHIP}	Device differential uniformity $D_{CHIP} = \text{ABS}(I_{COL_MAX} - I_{COL_MIN})/I_{AVG2}$, and $I_{AVG2} = (I_{COL_1} + I_{t0} + I_{COL_128})/128$			5		%
I_{BR1}	Maximum brightness current	BRIGHT.MAX = 0 BRIGHT.BRIGHT = 127		250		μA
I_{BR2}	Maximum brightness current	BRIGHT.MAX = 1 BRIGHT.BRIGHT = 127		500		μA

11.3.5 DC-to-DC Converter

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DRIVE_H}	External MOS gate: ON mode	$I_{DRIVE} = -20\text{mA}$	$V_{PP}-1$		10	V
V_{DRIVE_L}	External MOS gate: OFF mode	$I_{DRIVE} = 20\text{mA}$		100		mV
V_{DRIVE_CYCLE}	External MOS gate: turn ON duty cycle		0		80	%
R_{VHIGH_ON}	Internal MOS impedance: during Ton	$I_{VHIGH} = 20\text{mA}$	0	50		Ohm
Efficiency				80		%
V_{CAPA_HOLD}			0		20	V

11.3.6 Voltage Generator

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{COL_PRE}	Precharge power supply	Internal generator - $I_{COL_PRE} = -450\text{mA}$ - $I_{COL_PRE} = 100\mu\text{A}$ External generator		TBD TBD TBD	V_{PP}	V
V_{ROW_OFF}	Row-off power supply	Internal generator - $I_{ROW_OFF} = -450\text{mA}$ - $I_{ROW_OFF} = 450\text{mA}$ External generator		TBD TBD TBD	V_{PP}	V

12 Revision History

The following table summarizes the modifications applied to this document.

Revision	Description	Date
1.0	First Issue	28 October 2002
1.1	Updated diagrams. Addition of Table 2: Top Side (from left to right) , Section 10.1: Register Map .	18 November 2002
1.2	Modification of Figure 2: Die Description (Bump-side View) and addition of Table 2: Top Side (from left to right) , Table 3: Right Side (from top to bottom) , Table 4: Bottom Side (from right to left) , Table 5: Left Side (from bottom to top) and Table 6: Mechanical Dimensions .	21 November 2002
1.3	IDchip = 0101b Modification of Figure 28: Wrap Only - Example 2 , Figure 30: Wrap and Bounce - Example 2 , Figure 31: Row Driver Voltage Diagram , Figure 32: Column Driver Voltage Diagram , Section 5.2.1: Column Pre-charge/Discharge , Chapter 7: Power Supply Management - Powermizer™ and register PREDISDUR .	27 November 2002
1.4	IDchip = 0110b Modification of Figure 1: STV8102 Input/Output Diagram and Figure 2: Die Description (Bump-side View) . Update of Table 1: STV8102 Pad Description and Table 4: Bottom Side (from right to left) . Minor updates in Chapter 2: Bus Interfaces on page 16 . Modification of Figure 37: Power Supply Management Block Diagram . Update of Chapter 9: STV8102 Configuration and Chapter 10: Control and Status Registers Description on page 48 .	17 February 2003
1.5	Update of Figure 2: Die Description (Bump-side View) . Inclusion of Figure 3: COF Alignment and Die Positioning Marks . Update of pad placement and pad dimensions in Section 1.3: Lead Pad Reference Chart . Update of Figure 36: Self-adaptive Scanning Block Diagram . Other minor modifications.	17 April 2003
1.6	Update of Figure 2: Die Description (Bump-side View) .	29 April 2003
1.7	First issue for Cut 2.0 of the product Pins PATTERN_EN and PATTERN_SEL replaced by registers PATTERN_EN and PATTERN_SEL . Remark regarding functioning of screen panning introduced in Section 4.3 . Similar remark about screen saver functioning introduced in Section 4.4 . Table 19 modified to correspond to Figure 39 .	10 November 2004

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